





IEEE INDIA COUNCIL IEEE FELLOWS DIRECTORY

PREAMBLE

IEEE Fellow is a distinction reserved for select IEEE Members whose extraordinary accomplishments in any of the IEEE field of Interest are deemed fitting of this prestigious grade elevation. The total number selected in any one year does not exceed one-tenth of one percent (i.e. 0.01%) of the total voting institute membership.

On this celebrated occasion of "Azadi ka Amrit Mahotsav", IEEE India Council (IC) has planned to create a consolidated IEEE IC Fellow directory, a ready reckoner under the Professional Activities Committee (PACE) of IC. This shall also be accessible to members as well as public through our IC Website. Through this initiative, we plan to make members aware of the outstanding technical contributions made by IEEE Fellows/Life Fellows from India. This directory includes the IEEE Fellow Citation, brief bio and their technical contributions.

This Directory is regularly updated as and when we receive more information from remaining IEEE Fellows. We request IEEE Fellows who are not listed in this directory to kindly contact us, so that we can include their details too, which will help other members.

We are very sure this directory will help the Senior Members who plan for their elevation to Fellow grade. In addition to this, IC-PACE has also planned for Panel Discussions, TED Talks and Fireside chats with the listed IEEE Fellows. We hope this initiative will stimulate other IEEE Members to contribute towards the growth of the Nation such that India takes a leading position in technological advancement and Innovation by the time we celebrate "100 years of the Independence".

With Warm Regards



K R Suresh Nair Chair, IEEE India Council



Puneet Kumar Mishra Vice Chair (PA), IEEE India Council

1



IEEE Fellows from India (Partial list)



Anurag Kumar Affiliation: IISc Bangalore

IEEE Fellow Citation: For contributions to the performance analysis, optimization and control of communication networks and distributed computing systems

Bio: Prof. Anurag Kumar, B.Tech (1977) IIT Kanpur, PhD (1981) Cornell Univ., was a Member of Technical Staff in AT&T Bell Laboratories (1981-1988), before joining the Indian Institute of Science (IISc). He became a Professor in the ECE Department, in 1996, was the Director of the Institute during 2014-2020, and now, after superannuation, he is an Honorary Professor. He has published almost 200 peer reviewed papers in journals and conferences, in the area of communications networking and distributed systems. Prof. Kumar began his career in India at a time when the telecommunications revolution was just taking off and the Internet was just a fledgling network. He was one of the leaders of the ERNET project that established India's first nationwide Internet for academia. He was one of the early researchers in India in the mathematical approach to understanding and designing modern communication networks. He has led the authorship of two major textbooks that have been used around the world.

Recognitions: 1977 President's Gold Medalist in IIT Kanpur; IISc Alumni Award for Excellence in Engineering Research for 2008; elected Fellow of the IEEE, the Indian National Science Academy (INSA), the Indian National Academy of Engineering (INAE), the Indian Academy of Science (IASc), and The World Academy of Sciences (TWAS); 2015 Vasvik Award for Information Technology; 2017 IEI-IEEE Award for Engineering Excellence. Area editor (2005-2009) for the IEEE/ACM Transactions on Networking; on its steering committee from 2010-2014. J.C. Bose National Fellowship, awarded by the Department of Science and Technology, for the period 2011-2021.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Dr. Anurag Kumar has made important contributions to a range of problems in the stochastic modeling, analysis and optimization of resource sharing in communication networks and distributed computing systems. He has successfully applied research results to several important industrial problems. In addition, he has played a leading role in the setting up and operation of the first major packet-networking project in India. The following are a few of his contributions that were reported at the time of his nomination for the IEEE Fellowship.

In the area of Asynchronous Transfer Mode (ATM) networks, popular in the 1990s, he developed a distributed max-min fair rate allocation technique. This algorithm is based on the distributed computation of certain link parameters at all the network links, and the distributed update of the

3

source rates by means of control packets. This algorithm was implemented by Nortel Networks, and was patented (US Patent No. 6,597,662).

His analytical work on the Internet's TCP protocol in the mobile radio environment showed that, because of wireless losses and coarse time-outs, the throughput performance severely degrades for packet error rates more than 1%. Dr. Kumar also showed that, for given error rates, the TCP throughput performance improves as the errors become more bursty. This work has become a standard reference in the literature. In another contribution, he has shown, via novel stochastic modeling, that TCP controlled traffic in the closed loop need not lead to large queues even though the input traffic is long range dependent, thus establishing an important counterpoint to earlier research on the behavior of a buffer with long-range dependent input.

In the context of traffic controls in high speed networks, he formulated the state feedback delay problem in queuing control as a partially observed controlled Markov Chain, which led to novel structural results for the optimal policies. One of the results was that, in the problem of routing to one of two queues with information delay of one slot, the optimal policy is to allocate an arrival to the queue with the smaller expected queue length. This was shown to be not optimal for larger information delays. These results were among the first of their kind.

Dr. Kumar designed the overload control strategy that was implemented in the digital switching system developed by C-DOT (Centre for Development of Telematics); this system played a key role in the expansion of the Indian wireline telephone network. Dr. Kumar led the nationwide ERNET (Education and Research Network) project team at the Indian Institute of Science, and introduced the ideas of network performance, traffic measurement and systematic network management. An outcome was the NETMASTER system, for quality of service management at an Internet access link; this technology was purchased by Nextera Technologies, and developed into a commercial product, NeteraBM.

Dr. Kumar is the lead author an advanced level textbook titled ``Communication Networking: An Analytical Approach," which filled a commonly perceived void, and has been adopted as a text or reference in major universities in the West and in the East.



Ashok Jhunjhunwala Affiliation: IIT Madras

IEEE Fellow Citation: For leadership in development of cost-effective telecommunications in remote areas

Bio: Ashok Jhunjhunwala, Institute Professor at IIT Madras, President, IITM Research Park, IITM Incubation Cell and RTBI, did his B.Tech degree from IIT Kanpur and MS and PhD from University of Maine, USA and was a faculty at Washington State University, USA for a year and half before joining as a faculty at IIT Madras in 1981. In 2017-18, he was on sabbatical from IITM and was Principal Advisor to Minister of Power, MNRE, and Railways, Government of India, New Delhi.

Dr. Jhunjhunwala was conferred Padmashri, Shanti-Swarup Bhatnagar Award, Vikram Sarabhai Research Award, H. K. Firodia Award, Silicon India Leadership Award, Millenium Medal at Indian Science Congress, UGC Hari Om Ashram Award, IETE's Ram Lala Wadhwa Gold Medal, JC Bose fellowship, Bernard Low Humanitarian Award, "Dronacharya and Lifetime Achievement Award by TIE, Chennai among many others. He is fellow of IEEE, INSA, NAS, IAS, INAE and WWRF and a member of National Academy of Engineering (NAE), USA. He has also been conferred honorary doctorate by University of Maine and Blekinge Institute of Technology, Sweden.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Jhunjhunwala is considered a pioneer in nurturing Industry-Academia interaction in India towards R&D, Innovation and Product Development. He conceived and built India's first university affiliated business park (IIT Madras Research Park) to promote Industry-Academia R&D collaboration. TIE conferred him the title of Dronacharya for his contributions to the cause of entrepreneurship, as he incubated and nurtured more than 240 companies at IIT Madras. He heads the IITM Incubation Cell and Rural Technology and Business Incubator (RTBI). He leads TeNeT group, which has worked closely with industry to create innovative affordable products in sectors like telecom, banking, energy and electric vehicles.

Dr. Jhunjhunwala has been Chairman and member of various government committees and has been on boards of several education institutions in the country. At the same time, he has been on the boards of a number of public and private companies and has driven comprehensive changes, especially in the areas of technology, in these companies. He was on the boards of State Bank of India, Bharat Electronics Ltd, HTL, NRDC, IDRBT, VSNL and BSNL as well as in Tata Communications, Mahindra Electric, Sasken, Tejas Networks, TTML, Intellect and Exicom. He was on the board of BIRAC and the Chairman of Technology Advisory Group of SEBI. Also, he is currently part of RBI Innovation Hub and Chairperson in IIIT Kottayam and College of Engineering, Trivandrum, Kerala.

5



B L Deekshatulu

Affiliation: Ex-IISc Bangalore / NRSC Hyderabad IEEE Fellow Citation: For Technical Leadership in the development of Remote sensing and Image Processing technologies, and their successful implementation in Natural resources utilization in India

Bio: B L Deekshatulu , BSc (engg),M E, Phd, was a professor IISc (Bengalore),Director NRSA Hyderabad, Director CSSTEAP (UN) Dehradun, Visiting Professor UoHyd, Distinguished Fellow IDRBT Hyderabad. He retired as "Distinguished Scientist" (Secretary grade- Govt. of India) & Director NRSA in October 1996. He was responsible for upbringing of National Remote Sensing Agency (now NRSC) in all its facets, and for executing National and State level projects in many disciplines of Remote Sensing applications. He has over 160 research publications, guided 22 Ph.Ds and over 80 MTech. student dissertations. He visited 27 countries in the world. His current interests are Data Analysis, Digital Image Processing, Machine Learning and Neural Networks.

He is Fellow of 15 Scientific and Engineering Academies including Fellow IEEE (USA), Fellow THE WORLD ACADEMY OF SCIENCES (ITALY), Distinguished Fellow IETE, FNAE, FNA, FNAc, FASc, FNAAS, Distinguished Fellow of Astronautical Society of India. Hon. Member Asian Assoc. for Remote Sensing, Japan, Hon. Fellow ISRS. He is mentioned as "Living Legend in Indian Science" in Current Science Journal, 25 June 2014. He has won several awards besides Sir M Visweswaraya Award, Padmasri, Brahm Prakash Medal, Om Prakash Bhasin award, Bhaskara Award, National Award from MOES India, Distinguished Alumni Award (IISc), ISRO outstanding Achievment award, Boon Indrambarya Gold Medal(Thailand), Chen Shupeng Award (CCNCRS & AARS, Taipei), etc.

Dr. Deekshatulu was IEEE section Chair Hyderabad 1984-85. Dr. Deekshatulu has also contributed in the establishment of CSA Dept. at IISc Bengaluru, ADRIN and INCOIS organizations at Hyderabad. He is a great organization builder and a researcher.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

At IISc Banglore, Dr. Deekshatulu contributed to seeding and growth of control systems in all its aspects, both by way of research publications and by introducing ME level subjects such as Nonlinear Control, multi variable, adaptive optimal control, pattern recognition, bio control, etc. Control activities emerged from here. He planned and designed lab experiments in control using the Servo Analyser and CRT circuitry.

Prof. Deekshatulu started several new initiatives and starting of the M.E. program in Applied Electronics & Servo mechanisms, at IISc., Bangalore. It was a timely initiative when India was launching its rockets and missile program and also when ISRO was starting the space science program. He has also contributed a great deal in the establishment (initial stages) of School of Automation at IISc., Bangalore. It was the first interdisciplinary department drawing people from Electrical Engineering, Electronics and Communication Engineering, Mechanical Engineering, Aerospace systems, Computer science and Mathematics.

6

He Designed and fabricated, for the first time in India, at IISc Bangalore, a Gray scale Drum Scanner for scanning of pictures for Computer Picture Processing

He organized team within NRSA to carry out first ever forest cover mapping (suggested by Prof Satish Dhawan) using two time periods(1972-75 and 1980-82) of datasets. Ultimately the technology was accepted as a scientific tool to monitor forest cover. Today Forest Survey of India (FSI), an organization under Ministry of Environment and Forest, provides biennial assessments of forest cover using this technology. The implementation of this project opened up requirement of many new national level projects viz., wasteland, groundwater, land use and integrated Mission for Sustainable Development & Watershed Planning with the funding support from user ministries under National Natural Resource Management System (NNRMS). He motivated scientists to undertake research in different areas to develop newer applications in the fields of agriculture, earth sciences, oceanography and water resources. He built up a program in different thematic areas to address disasters like floods, drought, cyclone, forest fire and landslides. These areas subsequently evolved as a major initiative for operational service.

During mid-80's ISRO planed its own Indian Remote Sensing Satellites and launched its first satellite IRS-1 in March 1988. It is here Prof. Deekshatulu brought in a new era of change by upgrading NRSA earth station to receive the IRS series satellite datasets and provided high quality of diverse satellite products to user community in different application areas. NRSA developed systems, software to process satellite data, quality products with increasing volume and speed requirements. He spearheaded the effort for preparing real time products on potential fishing zone and disseminated relevant information to the fishermen of east and west coast of India.Some of the new areas which got evolved during his leadership are: Waste land development, Identifying agriculture crop types, acreage and yield estimation; identification of saline/alkaline soils (over irrigated areas)and their monitoring;, mapping of potential groundwater areas through geological fractures/lineaments, detecting and monitoring forest fires, detection of oil slick's in oceans surfaces, estimating irrigation efficiency in command areas,)estimation of snow melt run-off in the Himalayas rivers, mapping areas affected by floods and making damage assessment, cyclone monitoring and crop damage assessment after the landfall and a host of other applications of very practical relevance.



B Sundar Rajan

Affiliation: IISc Bangalore IEEE Fellow Citation: For contributions to high performance and low complexity space-time code designs for wireless communication systems

Bio: Received the B.Sc. in mathematics from Madras University, B.Tech in electronics from Madras Institute of Technology and the M.Tech and Ph.D. in electrical engineering from the IIT Kanpur; Was a faculty member with the Department of Electrical Engineering at IIT Delhi, from 1990 to 1997 and joined IISc in 1998, where currently is a Senior Professor. During 2004-05, he was with Beceem Communications Pvt. Ltd., as Distinguished Member of Research Staff, on leave from IISc.Fellow, IEEE; J.C. Bose National Fellow (2016-2025); Fellow of: Indian National Science Academy (INSA),Indian National Academy of Engineering (INAE),Indian Academy of Sciences (IASc), National Academy of Sciences, India (NASI), Institution of Electronics and Telecommunication Engineers (IETE) India; Was an Editor of the IEEE Communications Letters , IEEE Transactions on Information Theory and IEEE Transactions on Wireless Communications.

Recipient of IEEE Wireless Communications & Networking Conference (WCNC) 2011 Best Academic Paper Award, Khosla National Award for the year 2010 from I.I.T. Roorkee, Prof. Rustum Choksi award by I.I.Sc., for excellence in research (Engineering) for the year 2009 and IETE Pune Center's S.V.C. Aiya Award for Telecom Education in 2004; INAE Chair Professor during 2010-12; Served as Technical Program Co-Chair of the IEEE Information Theory Workshop (ITW 2002) held in Bangalore; Member of American Mathematical Society.

Primary research interests include MIMO signal processing & algorithms, Space-time coding for MIMO channels, Coding for multiple-access and relay channels, Interference alignment, Wired & wireless network coding, Index Coding, Coded Caching and Coded Computation with applications to Machine Learning, D2D and Vehicular Communications (V2X, V2V).

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Multiple Input Multiple Output (MIMO) communication systems refer to wireless communication systems transmitting with more than one transmit antenna and/or receive with more than one receive antenna. Such multi-antenna communication systems have been shown to have large capacity to transmit information compared single antenna communication systems. To realize and exploit this large capacity in practice one needs to employ good (efficient) codes at the transmitter side and good (efficient) signal processing algorithms at the receiver side. The codes used in such multi-antenna systems are known as space-time codes. During 2001-2010, along with several PhD students, space-time codes that can give high performance and space-time codes that have low decoding complexity and hence are suitable for implementation were developed in IISc under my supervision. Some of the codes developed have been accepted as part of the international standards like IEEE WiMax. These works resulted in a good number of papers in IEEE Transactions on Information Theory and IEEE Transactions on Wireless Communications triggering large number of follow-up works by other researchers in MIMO and resulting in large number of citations. For these contributions, he was elevated to IEEE Fellow Grade in 2014.

8



Affiliation: ISI Kolkata IEEE Fellow Citation: For contributions to Interconnection Networks and Parallel Algorithms

Bhabani P Sinha

Bio: Professor Bhabani P. Sinha joined the faculty of Electronics Unit of the Indian Statistical Institute (ISI), Calcutta in 1976, where he became a Professor in 1987. He served as the Head of the Advanced Computing and Microelectronics Unit (1993-2010) and Dean of Studies of ISI (2010-12). He was an Indian Space Research Organization (ISRO) Chair Professor in IIT Kharagpur (2000). After superannuation from ISI, since July 2017, he has been appointed as a Distinguished Professor in Siksha 'O' Anusandhan University, Bhubaneswar, India. He was an Alexander von Humboldt fellow of Germany. He received many awards and honors in recognition of his excellent academic performance and outstanding research contributions, the most notable of which include: i) M.K. Singal Memorial award from the Indian Science Congress Association in 2012 for his significant and lifetime contributions to the development of science and technology, ii) HomiBhaba award of the University Grants Commission, India (1998) for outstanding contributions to applied sciences, iii) Ram Lal Wadha Medal from the Institution of Electronics and Telecommunication Engineers, India for outstanding contribution in electronics and telecommunication engineering (2012), iv) Faculty Excellence award of Clemson University, USA (2002), and v) Eminent Engineer award from the Institute of Engineers, India (2008). He is a Fellow of IEEE, Indian National Academy of Engineering, National Academy of Sciences, India, Institution of Electronics and Telecommunications Engineering and West Bengal Academy of Science and Technology. His research interests include computer architecture, algorithms, parallel and distributed computing, mobile communication and wireless networks.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

- 1. Introduced the Multi-Mesh network architecture for parallel processing. The network topology of Multi-Mesh is based on using n⁴ processors with each processor being connected only to four other processors, resulting to a diameter of only 2n. On this architecture, various arithmetic operations, Lagrange's interpolation for numerical computing, sorting, etc. can be efficiently implemented for very fast parallel computation of all these operations.
- 2. Introduced other very efficient static network architectures including generalized hypercube connected cycles (GHCC) and twisted hypercubes, which are very suitable for parallel processing.

9

- 3. Proposed a number of fast parallel algorithms, e.g., an O(log n) parallel algorithm for multiplication of binary numbers with a scheme for its VLSI implementation, an O(n log n) parallel algorithm for computing all-pair shortest paths in a graph having n vertices, sorting, n⁴ elements in O(n) time, computing the discrete Fourier transform (DFT) coefficients of n⁴ points in O(n) time, etc.
- 4. Proposed an elegant concept of series folding which can be successfully applied for evaluating infinite series for arctan (x), e^x, log x, sin x, sinh(x), etc. corresponding to any value of the argument x, by computing a very small, e.g., 3 to 4 terms of the infinite series, by suitable transformations of the argument x. As a result, this concept of series folding leads to extremely fast evaluation of the above functions without compromising the accuracy.



Bhargab Bhattacharya Affiliation: ISI Kolkata IEEE Fellow Citation: For contributions to test and design of digital integrated circuits

Bio: Bhargab B. Bhattacharya had been on the standing faculty of Indian Statistical Institute, Kolkata, during 1982 – 2018. After his retirement, he served as Distinguished Visiting Professor of Computer Science & Engineering at Indian Institute of Technology Kharagpur, for more than three years (2019 – 2022). He received the B.Sc. degree in Physics from the Presidency College, Kolkata, B.Tech. and M.Tech. degrees in Radiophysics and Electronics, and the PhD degree in Computer Science, all from the University of Calcutta. He served as Visiting Professor at the University of Nebraska-Lincoln, and Duke University, USA, University of Potsdam, Germany, Tsinghua University, Beijing, China, and Kyushu Institute of Technology, Iizuka, Japan. His research area includes digital logic testing, and electronic design automation for integrated circuits and microfluidic biochips. He has published more than 400 technical articles and he holds ten US patents.

Dr. Bhattacharya is a Fellow of the Indian National Academy of Engineering and a Fellow of the National Academy of Sciences (India). He was the recipient of ISA TechnoMentor Award (2008) and IEI-IEEE Joint Award for Engineering Excellence (2018).

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

- Settled several theoretical and practical challenges concerning VLSI Design Flow: Anomalous behavior of stuck-at faults in logic circuits (Proceedings of the IEEE, 1983); inadmissible class of faulty functions (IEEE Trans. Comput. 1985); geometric peculiarities in VLSI layout design (DAC 1992); parity testability of logic circuits (IEEE Trans. Comput., 1989); bounds on testdata compression for IC chips (IEEE Trans. CAD, 2000);
- Biometric chip designed for fingerprint recognition (patented by Indian Statistical Institute and Intel Corporation) - US Patent # 7,359,532 (2008), US Patent # 7,136,515 (2006), US Patent # 7,027,649 (2006), US Patent # 6,795,592 (2004), US Patent # 6,681,060 (2004).



Bhuvaneswari Gurumoorthy Affiliation: Mahindra University, Hyderabad/IIT Delhi IEEE Fellow Citation: For contributions in design and development of improved power quality converters for variable frequency drives and switched mode power supplies

Bio: G. Bhuvaneswari is currently a professor in the Department of Electrical and Electronics Engineering at Mahindra University, Hyderabad, India. She accepted this position in March 2021, after serving as a faculty member in the Department of Electrical Engineering for over two decades at the Indian Institute of Technology Delhi, India. Early in her career she also worked for a few years in the electrical utility company ComEd, Chicago, Illinois, USA.Prof. Bhuvaneswari's research is in the area of power electronics, machines and drives. She is particularly interested in all the related application areas like power supply, power quality, HVDC transmission, electric drives, electric vehicles, battery charging and renewable energy. She has published over 200 papers based on her research in national and international journals and conferences.

She was the founder secretary and treasurer of IEEE PELS-IES Delhi Chapter in 2006. She also served as its Chair during 2010-2011 and 2017-2018. She is the associate editor of IEEE Journals of Emerging and Selected Topics Power Electronics as well as Industrial Electronics.

Prof. Bhuvaneswari is an elected Fellow of the National Academy of Engineering, USA "for contributions to advancement of power converters to improve power quality, and leadership in using advanced technologies for education". She is also an elected Fellow of IET-UK (2014), INAE (2013), IETE (2005), and IE (I) (2007). She received the IEEE-PES Wanda Reder Pioneer in Power Award in 2018 for contributions to educating and inspiring young women power engineers.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

One of the two most significant contributions of Prof. Bhuvaneswari is - Power quality improvement using multipulse AC-DC converters and Power factor corrected (PFC) converters for variable frequency drives and switched mode power supplies (SMPSs). She is one of the pioneering researchers to use multipulse converters for adjustable speed induction motor drives of medium capacity. She has also used improved power quality converters successfully for improving the power quality indices of SMPSs at the utility interface. She has designed and developed various multipulse converters, multiphase systems and ripple reinjection techniques to reduce supply current distortions to acceptable levels designated by the international power quality standards. There are over 300,000 mobile towers in India paying an electricity bill of Rs.40 million per month that utilize SMPSs for charging the batteries. Prof. Bhuvaneswari's research findings will impact energy conservation and

power quality aspects of these telecom tower power supplies appreciably. Besides, she has used the concept of modular converters effectively wherein the auto-connected transformer is completely eliminated; yet, significant power quality improvement is achieved using PFC technique. Both these techniques result in remarkable power quality improvements in front end AC-DCconverters for variable frequency drives, UPSs, industrial processes like heating, melting and welding and for renewable energy systems. She improved the reliability and cost-effectiveness of the multiout put SMPS for personal computers by making use of single-stage and two-stage DC-DC converters to regulate the output voltages. She used a weighted error approach to regulate various outputs and current mode control to improve the power quality at the utility interface. Her contributions in improved power quality converters have resulted in more than 20 IEEE journal publications with the total citations being 1000 with an h-index of 16 (Google Scholar). This has also resulted in three patents.

Prof. Bhuvaneswari's second important technical contribution is the design and development of a new shunt active power filtering algorithm namely, "Icos phi" algorithm,

that functions even in distorted and unbalanced supply conditions. This allows the power source to supply only the real fundamental component of current; so, reactive, unbalanced and harmonic components are fully compensated for by the active power filter, irrespective of distortions and unbalance in the supply voltages. This technique is used for current balancing across the windings of a three-phase self-excited induction generator supplying a single-phase load in a stand-alone configuration driven by pico/ micro hydro turbines. In remote locations, where power grid is unavailable, standalone power generation is the only means for having access to electricity. Thus, the nominee's work will support making an off-the-shelf three-phase induction generator supply electricity to single-phase loads in remote locations, without getting overheated. Prof. Bhuvaneswari is in the task force that is instrumental in creating power quality standards in India. She is closely working with International copper promotion council in "Asia Power Quality Initiative" towards formulating power quality standards as a part of Bureau of Indian Standards. Her research endeavors have propelled her to be nominated as an expert member by the President of India for the Solar power Energy Sector committee whose vision is to provide electricity to one and all in the country by 2020.



Bijnan Bandyopadhyay

IIT Jodhpur IEEE Fellow Citation: For contribution to discrete-time, multirate rate, output feedback sliding mode control

Bio: Bijnan Bandyopadhyay received his B.E. degree in Electronics and Telecommunication Engineering from the University of Calcutta, Calcutta, India in 1978, and Ph.D. in Electrical Engineering from IIT Delhi, India in 1986. In 1987, he joined the Systems and Control Engineering group, IIT Bombay, India, as a faculty member, where he has served upto 2021. In 1996, he was with the Lehrstuhl fur Elecktrische Steuerung und Regelung, RUB, Bochum, Germany, as an Alexander von Humboldt Fellow. He was awarded Distinguished Visiting Fellow by the Royal Academy of Engineering, London in 2009 and 2012. Professor Bandyopadhyay is a Fellow of: IEEE, INAE, NASI and IASc. He has 400publications which include monographs, book chapters, journal articles and conference papers. He has guided 40 Ph.D. theses. His research interests include the areas of multirate output feedback based discrete-time sliding mode control, event-triggered sliding mode control and nuclear reactor control. Prof. Bandyopadhyay served as Co-Chairman of the International Organization Committee and as Chairman of the Local Arrangements Committee for the IEEE ICIT, India, in 2000. He also served as one of the General Chairs of IEEE ICIT conference,, India in 2006. Prof. Bandyopadhyay has served as General Chair for IEEE International Workshop on VSSSMC, 2012. Prof. Bandyopadhyay has served as Technical Editor of IEEE/ASME Transactions on Mechatronics, Associate Editor of IEEE Transaction on Industrial Electronics and currently serving as Associate Editor IET Control Theory and Application. Prof. Bandyopadhyay has been awarded IEEE Distinguished Lecturer of IEEE IES society in 2019.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Bandyopadhyay is an internationally recognized researcher in Control system for more than last 35 years. He has made fundamental contributions to the theory of discrete time sliding mode control using multi-rate output feedback. His research findings are breakthroughs as a complete solution for discrete time sliding mode control, using output feedback was not available. More importantly due to increase in use of digital signal processor, digital control algorithms are very useful from the practical point of view. Hence his results address and remove a bottleneck for the application of theory to real world discrete time sliding mode control. He is recognized as a main contributor in the field of 'Discrete time sliding Mode control using output feedback(DSMC). His research paper in IEEE Trans.(IE) and monograph in LNCIS, Springer are the first to address this topic in control literature. He has been awarded IEEE Fellow for this citation in 2018. After his work many researchers started to do research in this area. He is instrumental to initiate and promote research in sliding mode control in India and in this process he guided 40 Ph. d. theses at IIT Bombay out of which 30 theses are on sliding mode control.



Chandan Chakraborty IIT Kharagpur

IEEE Fellow Citation: For contributions to estimation techniques and control of induction machine and drive systems

Bio: Chandan Chakraborty received B.E and M.E degrees in Electrical Engineering from Jadavpur University in 1987 and 1989 respectively and Ph.D degrees from Indian Institute of Technology Kharagpur and Mie University, Japan in 1997 and 2000 respectively. Presently, he is a professor in the Department of Electrical Engineering and Associate Dean, Sponsored Research & Industrial Consultancy, Indian Institute of Technology Kharagpur. His research interest includes power converters, motor drives, electric vehicles and renewable energy.Dr. Chakraborty was the Lead of the UK-India project on Reliable and Efficient System for Community Energy Solution (RESCUES). Currently he is the India side Lead of UKICERI, a consortium of multi institutes from India and UK on clean energy research initiatives with IIT Kharagpur as the Lead institute from the India-side. Dr. Chakraborty received the JSPS Fellowship to work at the University of Tokyo during 2000-2002. He has also received many awards/recognitions including IEEE Bimal Bose Energy Systems Award in 2019, Avinash Gupta Chair Professor Award in 2021 etc. He has regularly contributed to IES conferences such as IECON, ISIE and ICIT as technical program chair/track chair. He is one of the founding members to conceptualize and start a new series of IEEE conferences entitled IESES (IEEE International Conference on Industrial Electronics for Sustainable Energy Systems). He has served as Associate Editor in IEEE Transactions on Sustainable Energy, IEEE Journal of Emerging and Selected Topics in Power Electronics, IEEE Transactions on Industrial Electronics and IEEE Industrial Electronics Magazine. He is the Founding Editor-in-Chief of IE Technology News (ITeN), a web-only publication for IEEE Industrial Electronics Society. He has served as a Co-EIC of IEEE Transactions on Industrial Electronics during 2018-19. Presently he is the Editor-in-Chief of IEEE Journal of Emerging and Selected Topics in Industrial Electronics (JESTIE). He is a Fellow of IEEE and Indian National Academy of Engineering (INAE).

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Chakraborty's major contributions are in the areas of (i) power electronics, (ii) industrial drives and (iii) electric machines. In power electronics he proposed new topological configurations and control techniques of multi level converters, active power filters/static VAR compensators and resonant converters. His pioneering contributions in industrial drives include proposal of new series of adaptive controllers for speed and parameter estimation of induction motor drives and development of fault tolerant controllers. In electric machines, he has for the first time shown the influence of parameter variation on parallel-operated self-excited induction generators.

In motor drives, he has pioneering contributions on the control and parameter estimation of induction motor (IM) drives. He has proposed new ideas to eliminate the speed sensor of vector controlled drive increasing robustness and reducing cost. His major contribution is to propose new model reference adaptive controllers (MRAC) using reactive power (Q) as the functional candidate. Instantaneous and steady state Q are used to form the MRAC. The proposed algorithm is only influenced by rotor time constant and in fact by modifying the algorithm he has shown that rotor resistance may be estimated in case speed signal is available. A four quadrant control is demonstrated using ANN. This is a unique example where classical control and soft computing are properly hybridized for enhancing stability of a system. He has recently proposed a new candidate X (which is the outer product of terminal voltage and current) for such adaptive controllers. X has no physical significance unlike active (P) or reactive (Q) power. It has been shown that X-based controllers are inherently stable in all the four quadrants of operation and demonstrate excellent performance at low operating speed. Very recently he has proposed a series of model reference adaptive controllers (MRAC) those can work stably in all the four quadrant of operation. In particular, he has introduced a new configuration of Q-based MRAC and proved it's supremacy over all available configurations. His work on efficiency optimization is a hybrid technique of loss model and search based approaches. This has the merits of fast convergence and immunity to parameter variation. Recently, he has proposed a new current estimation technique (for the vector controlled drives) that is independent of inverter switching states, does not require an additional sensor and is independent of parameter variation. Utilizing the speed and current estimation techniques and introducing a new phasor rotation concept, he has proposed a unique fault tolerant controller that can operate even in case of multiple sensor failures.

In early stage of his career, Chandan worked on induction generators. He used inverse-gamma model of the machine to explore the limiting behavior of self-excited induction generator in a systematic manner. He has for the first time investigated the load sharing of individual generators when operated in parallel and have demonstrated that rotor resistance is the most important parameter for such machines. He has also proposed a simple test for the existence of self-excitation. This method is later published in book and is widely used.

16

D P Kothari Affiliation: VNIT Nagpur



Bio: Dr. D. P. Kothari obtained his BE (Electrical) in 1967, ME(Power Systems) in 1969 and Ph.D. in 1975 from BITS, Pilani, Rajasthan. From 1969 to 1977, he was involved in teaching and development of several courses at BITS Pilani. Earlier Dr. Kothari served as Vice Chancellor, VIT, Vellore, Director in-charge and Deputy Director (Administration) as well as Head in the Centre of Energy Studies at Indian Institute of Technology, Delhi and as Principal, VRCE, Nagpur. He was visiting professor at the Royal Melbourne Institute of Technology, Melbourne, Australia, during 1982-83 and 1989, for two years. He was also NSF Fellow at Perdue University, USA in 1992. He also taught at Melbourne University Australia for one semester in 1989.

Dr. Kothari is a Fellow of National Academy of Engineering, Indian National Academy of Science, Institution of Engineers, IEEE, Hon. Fellow ISTE and IETE. He has received 81 awards till now, including the National Khosla Award for Lifetime Achievements in Engineering (2005) from IIT, Roorkee. The University Grants Commission (UGC), Government of India the UGC National Swami Pranavandana Saraswati Award (2005) in the field of education for his outstanding scholarly contributions.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Research Areas of Interest – Electrical Power System Engineering with special interest in System Analysis, Load Flow, Economic Load Dispatch, Computer Control and system Optimization, Reliability, Water Management, Stability, Energy Conservation, Minimum Emission Dispatch, Security and Contingency Analysis, Unit Commitment, Maintenance scheduling, Planning and Management of Rural Energy Systems, Urban Energy Planning, Conventional & renewable energy sources.

- 1. Authored 73 books, guided 57 PhDs and 68 M.Tech theses, 840 research papers, 8 patents & 30 projects and Consultancies.
- 2. Helped develop Engineering Curriculam in CD Cell, BUGS and BPGS etc.,
- 3. Chaired and participated in IIT Delhi Senate and took many important academic and administrative decisions
- 4. Carried out many educational reforms, syllabus upgradation and implemented schemes-Practice School, Twinning Program, Fully Flexible Credit System (FFCS).

- 5. Have attended, presented papers and chaired technical sessions in India and abroad.
- 6. Helped many persons in writing Engineering Textbooks and reference books.
- 7. Deliverd 100 + webinars on several topics. Special Achievements
- 8. Unique diction of holding all the three positions- IIT Director, NIT Director, Vice Chancellor. -At 78 and with physical disability, there is no other faculty member who is still active in teaching, research, writing books etc.
- 8. Received 81 National and International awards.
- 9. Currently Adjunct Professor/ Distinguished Emeritus Professor/Visiting Professor in several universities and colleges such as Distinguished Professor Emeritus in Dept. of Electrical Engineering / Dept. Automation & Robotics, Prestige Institute of Engineering Management & Research, Indore, MP, Distinguished Emeritus Professor at Techno India NJR Institute of Technology, Udaipur & Adjunct Professor (Visitor & Advisor) at Tula's Institute, Dehradun. I am also Chairman Board of Governers, THDC Institute of Hydropower Engineering and Technology, Tehri, Uttarakhand.



Debatosh Guha Affiliation: University of Calcutta IEEE Fellow Citation: For contributions to microstrip and wideband dielectric resonator antennas

Bio: Debatosh Guha is a Professor in Radio Physics and Electronics, University of Calcutta. He is the former HAL Chair Professor of Indian Institute of Technology (IIT) Kharagapur and former Director of the Centre for Research in Nanoscience and Nanotechnology (CRNN), University of Calcutta. He is Abdul Kalam Technology Innovation National Fellow of the department of science and technology (DST), Govt. of India. He has made some fundamental contributions to antenna technology for the new generation radar and airborne applications. His techniques are being used in several industrial applications and by leading R&D Laboratories. More than 200 technical papers along with a couple of books published Wiley/IEEE Press are in his credit. His research contributions are frequently cited by others and featured in the recent editions of top text/handbooks in the antenna domain.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Fundamental Concepts Developed for Planar Antenna Engineering:

- 1. Debatosh Guha has made fundamental contributions to low-profile microwave and wireless antennas using printed circuit technology and low-loss ceramic based dielectric resonators with practical significances.
- 2. He introduced the concept of defected ground structure (DGS) integration technique to printed antennas (IEEE AWPL, 4, 455-458, 2005) and consistently developed the theory followed by experiments to attain the maturity to the level of industrial applications. He first enunciated small non-resonant type DGS beneath a circular microstrip antenna and explained how to weaken the unwanted higher-order modes and mitigate two severe issues commonly occurring in large radar arrays- (i) high cross-polarized radiation fields (IEEE AWPL, 4, 455-458, 2005) and (ii) mutual coupling among elements causing scan-blindness in radiation patterns (IEEE AWPL, 5, 402 405, 2006).
- 3. Debatosh has made original contributions to Dielectric Resonator Antennas (DRAs) especially by introducing unconventional radiation modes and multi-mode engineering. He addressed the physics behind controlling consecutive multi-mode resonances and changed the traditional concept of wideband or ultra-wideband DRA designs. That opened a more theory-based methodology using composite and hybrid configurations (IEEE TAP, 54, 2657-2662; 2006; IEEE TAP, 54, 3621-3628, 2006; IEEE AWPL, 5, 373-376, 2006). His research had introduced

a new and a truly useful radiating mode in cylindrical DRAs showing several attractive features (IEEE TAP, 60, 71-77, 2012). To establish its viability, he has developed integratable new feed configurations for the same (IEEE AWPL, 13, 15-18, 2014; IEEE TAP, 63, 433-438, 2015; IEEE TAP, 64, 1497-1502, 2016) which should lead to realizing antenna-on-chip in the near future.

Advanced Techniques and Applications:

- 1. Debatosh has developed advanced theory for microstrip antenna using composite substratesuperstrate combinations (IEEE TAP, 49, 55-59, 2001; IEEE TAP, 51, 1649-1652, 2003). Based on the same, he showed various ways to controlling effective aperture and input impedances (IEEE TAP,52, 2174-2178, 2004) and thus opened a new approach of microstrip antenna design for various applications (IEEE TAP,57, 3325-3328, 2009; IEEE APM, 52, 92-95, 2010).
- 2. After proposing the new DGS concept, he along with his students and collaborators, carried out extensive research to generalize the DGS theory by developing various shapes (IEEE AWPL, 8, 1367-1369, 2009; IEEE TAP, 60, 92-101, 2012) and geometry-independent universal configurations (IEEE TAP, 63, 2767-2772, 2015). These studies showed the way of enhancing the cross-pol suppression from 5 dB to the level of 13 dB. His technique adds no extra cost, weight, or volume to the antenna and hence appears to be the best suited one for airborne radars. The complete theory with technical details was first provided by Debatosh in an exclusive book chapter (Ch-13 in Microstrip and Printed Antennas, Wiley-UK, 2011). Later on, Wiley EEE Encyclopaedia incorporated this topic in 2013 edition. 'Defected Ground Structure Antenna' has grown as a new branch of activity as revealed by several thousands of classified documents generated since 2005. Several important practical applications were subsequently reported. Removal of scan blindness of radar antenna along with improved polarization purity is the most significant of them.



Gopakumar K. IISc Bangalore IEEE Fellow Citation: For contributions to design and control of multilevel converters

Bio: Dr. K. Gopakumar received his B.E. (Electrical Engineering, M.Sc. (Engg.)(E.E.) and Ph.D. (E.E.) from Indian Institute of Science, Bangalore. Dr. Gopakumar is currently a Professor at Department of ElectronicsSystems Engineering (DESE) - formerly known as the Centre for Electronics Design and Technology (CEDT), at I.I.Sc. He is also affiliated with the following professional societies: Fellow of the IEEE, Fellow of IETE (India), and Fellow of the Indian National Academy of Engineers (NAE). He is the winner of the prestigious IETE B. K. Bose Award for contributions to the area of power electronics and drives for high power applications, in 2008. Recipient of the Alumni(IISc) award in excellence in research award in2016. He is a Distinguished Lecturer of the IEEE Industrial Electronics Society. He also served as Co Editor-in-Chief of the IEEE Transactions on Industrial Electronics. He is the recipient of the IEEE -Eugene Mittelmann award in 2019

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Dr. Gopakumar's research has spanned three related but distinct areas in the broad area Power converters and Drives: (1) multilevel inverter structures for Induction motor (IM) drives with open-end winding structure for the motor. (2) Multiphase induction motor drives and (3) Space vector PWM control with simultaneously achieving common mode voltage elimination and DC link capacitor voltage balancing, using only the switching state redundancies, for multilevel inverter fed IM drives. He has made seminal contributions in each of these three areas and one of the pioneers in multilevel voltage space vector generations for IM drives with open-end winding structure and independent speed control of series connected multiphase IM drives, which has spurred interest in many other researchers leading to further interesting publications. The following is a description of his most creative research contributions in three areas of current research interest in power converters and drives, world wide.



Jayant R Haritsa

IISc Bangalore IEEE Fellow Citation: For contributions to the theory, design and implementation of data management systems

Bio: Jayant Haritsa is on the faculty of the Dept. of Computational & Data Sciences and the Dept. of Computer Science & Automation at the Indian Institute of Science, Bangalore, since 1993. He received a BTech degree from the Indian Institute of Technology (Madras), and MS and PhD degrees from the University of Wisconsin (Madison). He is a Fellow of ACM and IEEE, and of INAE, IASc, NASI and INSA. He is a Distinguished Alumnus of IIT Madras, and a recipient of the Swarnajayanti Fellowship, the Shanti Swarup Bhatnagar Award, and the Infosys Prize.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

An organic reason for the pervasive popularity of database systems is their support for declarative user queries, wherein the user only specifies the end objectives and the system takes on the responsibility of identifying the most efficient execution plan to achieve these objectives. A daunting challenge, however, is that this optimization process is computationally highly expensive since an exponentially large set of alternative plans must be evaluated and compared.

In 2002, Jayant Haritsa brought fresh hope to this classical problem by developing an ingenious machine-learning-based technique that drastically reduced the computational overheads while retaining plan quality close to the brute-force approach. This work opened a new area of research and is among the select few academic research papers to be hosted on SQL Summit, a highly-regarded database industry portal.

Then, in 2005, Jayant conjured up a radically fresh perspective on the foundations of query optimization by introducing and germinating the notion of "plan diagrams", a powerful visual metaphor for characterizing the behavior of modern query optimizers. Leveraging this metaphor, he developed the Picasso visualization platform which highlighted a variety of basic flaws in current optimizers, such as highly complex plan diagrams resembling "cubist-paintings", forcing database vendors to revisit their design principles. Through an imaginative plan-replacement algorithm, he established the unexpected and potent result that complex plan diagrams can be reduced to much simpler "anorexic" pictures featuring only a few plans, without materially affecting the query processing quality. A novel aspect of these replacement schemes is that they operate in the parametric-optimal space rather than the exponentially large plan search space, thereby ensuring computational efficiency.

Anorexic diagram reduction has a variety of practical performance benefits, and Jayant creatively used it in 2008 to address the long-standing problem of identifying robust plans that work well over large regions of the parameter space. He accomplished this through a novel mathematical characterization of plan cost functions, which lends itself to systematically identifying replacement plans that are organically robust. By proving the landmark result that replacement safety at the corners of the parameter space guarantees safety in the interior as well, he ensured efficiency in the computationally challenging identification process.

Then, in 2010, Jayant took a major leap forward by demonstrating how the above-mentioned desirable characteristics for query plans, which were predicated on off-line knowledge of the plan diagram, could be achieved dynamically for on-the-fly queries. This objective was realized through an innovative reworking of the core dynamic programming procedure that lies at the heart of query optimization, resulting in a database engine that directly generates anorexic and robust plan diagrams. Explicit evidence of the practicality of these ideas was demonstrated through incorporation in the PostgreSQL kernel.



K V S Hari Affiliation: IISc Bangalore **IEEE Fellow Citation**: For contributions to high-resolution signal parameter estimation

Bio: K V S Hari is a Professor in the Department of ECE, Indian Institute of Science, Bangalore. He holds a BE (ECE) degree from Osmania University, Hyderabad, MTech (Radar and Communication Systems) from IIT Delhi and PhD (Systems science) from U C San Diego and has been a visiting faculty at Stanford University and Affiliate Professor at KTH- Royal Institute of Technology, Stockholm. His research interests are in Signal Processing with applications to 5G wireless communications, radar systems, autonomous vehicles, neuroscience, and affordable MRI systems. He is a co-author of the IEEE 802.16 standard on wireless channel models. He was an Editor of EURASIP's Signal Processing (2006-16) and is currently the Editor-in-Chief (Electrical Sciences) of Sadhana, the journal of the Indian Academy of Sciences published by Springer. He is currently Chair, Standardisation Committee, Telecom Standards Development Society, India. He is a Fellow of IEEE. He is on the Board of Governors, IEEE Signal Processing Society as VP-Membership. More details at http://ece.iisc.ac.in/~hari

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Hari has made fundamental contributions to the performance analysis of Subspace Methods for Direction of Arrival (DOA) estimation such as MUSIC, Root-MUSIC and ESPRIT. Prior to the nominee's work, the performance metric for spectral methods, like Root-MUSIC, was not well understood. Hari's insight on the contributions of the radial and cross-radial errors in the roots of the underlying polynomial to the desired DOA estimates was crucial. This led to a wide range of results in performance of polynomial rooting based solutions to the DOA and spectral analysis problem. These solutions were also directly applicable to System Identification (SI) of linear systems.

Subspace methods (SM) have been widely applied in wireless communications, underwater acoustics, radar, meteorology, remote sensing, biomedical engineering and robot mechanisms. MIMO wireless channel models use SM to localise dominant scatters in azimuth and Elevation. In underwater acoustics, SM has been successfully applied to mode identification. Biomedicine uses SM to estimate Doppler spectrum of blood flow. Radar signal processing is another application for SM to estimate angular parameters. Spacecraft have used them to identify robot mechanisms. In all these applications, the error performance is a crucial requirement and the nominee's work has been central contribution in all these applications. The nominee's work has been cited in papers ranging from rheumatology, diabetes control, ocean biology and bridge design and also widely cited in classic textbooks on array processing and spectral analysis.

The other significant contribution of the nominee has been in the field of MIMO Wireless Channel Modeling. The earliest contributions on MIMO channel models came from the nominee, based on channel measurements at Stanford University. This work, carried out at Stanford University, resulted in the development of the Stanford University Interim (SUI) channel models. The SUI models captured the role of antenna height, pattern and spacing in MIMO propagation. At the time when this work was done, there were of course no MIMO channel sounders. The nominee played a key role in building simple measurement jigs. The measurements highlighted some interesting behaviour of real world MIMO channels. SUI models were very influential on all future MIMO wireless models. The first standardised MIMO model came from the IEEE 802.16 group and was based on the SUI models, when researchers from industry and academia collaborated on the effort. The nominee's contribution has been well cited by workers in academia and industry. The papers and IEEE standard document have been cited in several recent books. The models have also been incorporated in MATLAB Communications Toolbox 4.5. The nominee's work on wireless channel models has been fundamental to the development of standardised MIMO wireless models for WiMAX, LTE and WiFi, and thus been an important enabler of MIMO technology.



Karthikeyan M V Affiliation: IIT Roorkee/IIT Tirupati IEEE Fellow Citation: For contributions to high-power millimeter wave and terahertz sources

Bio: Prof. M.V. Kartikeyan received Master of Science and Ph.D. degrees specializing in Advanced Electronics & Radio Physics and Microwave Engineering from Banaras Hindu University and IIT-BHU, Varanasi, India, in 1985 and 1992, respectively. He was a Research Scientist with the Central Electronics Engineering Research Institute, Pilani, India, from 1989 to 2001. He was with Institutfuer Hochleistungsimpuls-und Mikrowellentechnik, Karlsruhe Institute of Technology, Karlsruhe, Germany (1996, 1998-2000, 2001-2003). He joined the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee (IITR), India, as an Associate Professor, in 2003, and elevated to Full-Professor in 2009. At present, he is working as a Professor in the Department of Electrical Engineering and Dean, Faculty Affairs at IIT-Tirupati on deputation since October 2020. He is the principal author of 5 books. He published more than 350 research papers in peer reviewed transactions/journals and conferences. His current research interests include high power millimeter wave and terahertz sources; RF Circuits, Antennas and Systems; Metamaterials and fractals; Computational Electromagnetics; and RF and microwave design with soft computing and machine learning techniques.

Prof. Kartikeyan is a Fellow of: IEEE (USA), Indian National Academy of Engineering, Institution of Engineering and Technology (UK), Institution of Electronics and Telecommunications Engineers, and Institution of Engineers. Prof. Kartikeyan is a recipient of the Hildegard-Maier Research Fellowship for Electrical Sciences of the Alexander von Humboldt Foundation (1998-2000) and the Alexander von Humboldt Research Fellowship (2001-2003, 2011, 2012).

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

- 1. Seminal contributions on 140-170 GHz megawatt class gyrotrons (both conventional and coaxial versions) working coherently with German collaborators, IHM/KIT, for more than two decades for plasma heating applications in experimental tokamaks, stellarators, and thermonuclear fusion reactors for global energy solutions. His works on the theory and design of high power gyrotrons has been treatised as a comprehensive text book on Gyrotrons which is studied worldwide in universities and research institutes by the research community working on gyro-devices. Additionally, he has significant contributions in the introduction of soft-computing techniques in the microwave domain (particularly for the design and optimization of microwave/millimeter-wave components).
- 2. Pioneered the complete design that lead to the successful development of the first Indian gyrotron operating at 42 GHz, 200 kW, CW, for the first indigenously developed experimental Tokamak in India.

26



Mayank Vatsa Affiliation: IIT Jodhpur IEEE Fellow Citation: For contributions to secure biometric recognition

Bio: Mayank Vatsa is a Professor and Professor-in-Charge of Corporate Relations with IIT Jodhpur, India, and an Adjunct Professor with IIIT-Delhi and IISER Bhopal. Since its inception, he is also the Project Director of the Technology and Innovation Hub on Computer Vision and Augmented & Virtual Reality under the National Mission on Cyber Physical Systems by the Government of India. His areas of interest are biometrics, machine learning, computer vision, and deep learning. He is a recipient of the Prestigious Swarnajayanti Fellowship from Government of India, NVIDIA Innovation Award, the A. R. Krishnaswamy Faculty Research Fellowship at the IIIT-Delhi, and several Best Paper and Best Poster Awards at international conferences. He is/was an Associate Editor of Information Fusion and Pattern Recognition, the General Co-Chair of IJCB 2020, and the PC Co-Chair of the ICB 2013, IJCB 2014, FG2021, AVSS2021. He has also served as the Area Chair of CVPR, AAAI, ICCV, ECCV conferences. From 2015 to 2018, he served as the Vice President (Publications) of the IEEE Biometrics Council where he led the efforts to start the IEEE TRANSACTIONS ON BIOMETRICS, BEHAVIOR, AND IDENTITY SCIENCE. He has also participated in several government initiative including designing biometrics Standards for e-Gov applications and DigiYatra.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Mayank has made several impactful contributions ranging from designing novel algorithms and datasets in biometrics, and Standards for national projects. There are many critical issues in designing a practical biometric system such as accuracy, computation speed, cost, and security. Among these, security of biometric data and system is of paramount importance. Mayank has pioneered in building novel approaches to secure biometric systems against attacks. He has contributed in designing watermarking based template protection schemes as well as spoofing and anti-spoofing mechanisms in biometrics. He was among the first researchers to present a large scale study on the effect of textured contact lenses on iris recognition. His work also focuses on crafting generalizable and computationally light-weight algorithms which are hard to fool (papers in IEEE BTAS 2016, ICPR 2016). Furthermore, his papers in WACV2020, IAPR/IEEE IJCB 2017, IEEE T-IFS 2016 also showcase that digital retouching and deepfakes affect face recognition performance. In the last few years, Mayank has extended this line of research and is working extensively on the security of deep learning based biometrics algorithms and proposing several algorithms and published them in top venues.

Several of his tools are being used by the user agencies while the related databases prepared by his team are being utilized by the researchers worldwide in developing next generation algorithms. He has prepared more than 40 databases related to face, fingerprint and iris modalities, including mainstream and newer challenging scenarios. He is among the very small group of researchers in the biometrics community who are just not database users but also creators. The list of databases prepared by him are available at http://iab-rubric.org.

He was involved in India's UIDAI project, the largest biometrics based national-ID project in the world. He has not only done the very first feasibility study for UIDAI, he has also contributed in writing the Biometrics Standards for Indian ecosystem. Additionally, an inspiring example of translating a research idea into a reality is his research on Drone based face recognition.

Neelesh B Mehta

Affiliation: IISc Bangalore IEEE Fellow Citation: For contributions to opportunistic selection in wireless communication systems



Bio: Neelesh B. Mehta is a Professor in the Department of Electrical Communication Engineering at the Indian Institute of Science (IISc), Bangalore. He received his B. Tech. degree from IIT Madras in 1996 and his Masters' and Ph.D. degrees from the California Institute of Technology, USA, in 1997 and 2001, respectively. From 2001 to 2007, he worked in the USA at AT&T Research Labs, Broadcom Corp., and Mitsubishi Electric Research Labs. His research focuses on the design, modeling, analysis, and optimization of current and next-generation wireless systems. He has participated in projects involving industries such as Boeing, Intel, British Telecom, Nokia, and Qualcomm, and government agencies such as MEITY, CEFIPRA, SERB, and DRDO. He is a Fellow of the IEEE, Indian National Science Academy (INSA), Indian National Academy of Engineering (INAE), and National Academy of Sciences India (NASI). He is a recipient of the IIT Roorkee's Khosla National Award in Engineering, Shanti Swarup Bhatnagar Award, Hari Om Ashram PreritVikram Sarabhai Research Award, DST-Swarnajayanti Fellowship, and NASI-Scopus Young Scientist Award. He is the Chair of the Steering Committee of the IEEE Transactions on Wireless Communications. He served on the Executive Editorial Committee of the IEEE Transactions on Wireless Communications during 2014-17 and was its Chair during 2017-18. He serves on ComSoc's Nominations and Elections standing committee, SERB's EECS PAC, and INSA's Sectional Committee V (Engineering and Technology). In the past, he has served on the Board of Governors of the IEEE Communications Society and the IEEE ComSoc awards committee.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Neelesh B. Mehta has contributed to the design, analysis, and optimization of wireless communication systems. He was an early pioneer in studying the fundamental new design trade-offs that arise in green, energy harvesting wireless networks. These networks circumvent the vexing problem of a limited network lifetime faced by conventional wireless sensor networks. He has worked on the design and analysis of distributed and scalable opportunistic selection algorithms. These include the widely used timer and splitting algorithms, which are fast, distributed, and scale well as the number of nodes increases. His work has led to new, computationally-efficient characterizations of the optimal structure of these selection algorithms. He has proposed new optimal criteria that specify the antenna or relay to select in cognitive radio systems. These differ from the ad hoc criteria proposed in the literature and outperform them. His work on opportunistic selection is relevant in several areas of



P.V.Ananda Mohan Affiliation: Ex-ITI Ltd. R&D&C-DAC IEEE Fellow Citation: For contributions to telecommunications technologies

Bio: P.V. Ananda Mohan received the B.Sc and M.Sc (Tech.) degrees from Andhra University, India, in 1965 and 1968, respectively and the Ph.D degree in electrical communication engineering from Indian Institute of Science, Bangalore, in 1975. He was with I.T.I. Limited R&D from 1973 till 2003 and later was with Electronics Corporation Of India Limited, Bangalore in R&D. He was later with Centre for Advanced Computing (CDAC), Bangalore as Technology Advisor from 2014 till 2020. His research interests are in the areas of VLSI design, VLSI architectures, Cryptography. He has published in these areas in refereed international journals and conferences. He has co-authored five books Switched Capacitor Filters: Theory, Analysis and Design with Dr. M. N. S. Swamy and Dr. V. Ramachandran (Prentice-Hall, 1995) and authored four more books Residue Number Systems: Algorithms and Architectures (Kluwer Academic, 2002), Current-Mode VLSI Analog Filters: Design and Applications (Birkhauser, 2003), VLSI analog Filters, Birkhauser 2012 and Residue Number Systems: Applications, Birkhauser 2016. He has published about 100 papers in refereed International Journals and Conferences. He is a reviewer for IEEE Transactions, IET Journals, CSSP etc.Dr. Mohan is a Life Fellow of IEEE (U.S.A), Fellow of IETE (India), and National Academy of Engineering. He was the Chair of IEEE CAS Chapter, Bangalore till 2020 from its inception. He was the Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS during 2000-2003. He is Editor-in-Chief of IETE Journal of Education and Associate Editor of Circuits, Systems and Signal Processing (CSSP), Birkhauser.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Dr. Anand has been publishing in the area of Active RC filters, VLSI implementations of Cryptographic algorithms since 1973. He was in telecom industry throughout working on development of Electronic Switching systems, Line cards for Exchanges, PCM filters He has developed encryption algorithms for Indian Armed Forces and implemented them in various products supplied by I.T.I. limited. He has published at that time three books (a) Switched-Capacitor filters for Prentice-Hall (London), (b) Current mode Signal processing for Birkhauser (Boston) and (c) Residue Number Systems for Kluwer Academic publishers. I was Associate Editor of IEEE Transactions on CAS and published quite few papers in IEEE Transactions, Proc.IEEE, Electronics Letters, AEU and presented papers at ISCAS at New Port Beach, Rome, Helsinki, San Jose. Portland, and Kyoto.



R. K. Shyamasundar Affiliation: IIT Bombay IEEE Fellow Citation: Pioneering Contributions to Logics of Programming

Bio: Prof. R.K. Shyamasundar is with the IIT Bombay, Mumbai where he is currently a INAE Distinguished Professor at Department of Computer Science and JC Bose National Fellow. He took his B.E. (Electrical Engineering) from University of Mysore, M.E. (Electrical Engineering) from Indian Institute of Science, Bangalore, and Ph.D. (Computer Science and Automation), from Indian Institute of Science, Bangalore. His principle areas of research are: Specification, Design and Verification of reactive and real-time systems, Programming Languages, Logics of programs, Formal methods, Computer and Network & Information Security. He has published widely and has more than 200 publications in refereed journals, conference proceedings, two monograph, several edited books, and holds several patents in US and India. He has given several invited talks at various conferences and has guided more than 35 Ph.D. students who are occupying leading positions in academia and industry. He is a Fellow of: IEEE, ACM, INSA, NASI, INAE, IASc, IETE, British Blockchain Association, and TWAS. He was awarded the 2014 SN Mitra award for excellence in research by the Indian National Academy of Engineering. He is Distinguished Alumnus of Indian Institute of Science, Bangalore.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

- a. Reactive and Real Time Systems: laid a foundation for a compositional specification and verification of a real-time distributed language using realistic parameters. It formed core for several lead ESPRIT projects. His pioneering work of Communicating Reactive Processes was the first to demonstrate the realization of complex verifiable systems through the unification of asynchrony and synchrony and has formed an integral part of complex system specification
- b. Concurrency & Logic programming: pioneered the exploitation of the inherent parallelism in specifications without foregoing safety in concurrent languages that has now a tremendous use in effective modeling and realization of multicore architectures. First adaptation of rewriting systems for establishing termination of Logic programs and lead the development of methodologies/tools that could establish the termination of Prolog compilers.
- C. Industrial Applications: Some notable systems developed and used in industry are (i) Object code validation system for Indian defence industry that also demonstrated such an application for debugging of optimized code and mobile code certification, (ii) Scalable verifiers through Computing Abstractions by Integrating BDDs and SMT Solvers, (iii) May Happen-in-Parallel Analysis for next generation programming languages such as X10,and (iv) protection of user managed memory in embedded systems.
- d. Cyber Security: Has built several systems for e-commerce including micro-payment systems, malware analysis systems, IDS systems etc. which are in use.



Ranjan K. Mallik Affiliation: IIT Delhi IEEE Fellow Citation: For contributions to channel characterization in wireless communication systems

Bio: Ranjan K. Mallik is a Professor in the Department of Electrical Engineering, Indian Institute of Technology Delhi. He received the B. Tech. degree from the Indian Institute of Technology Kanpur and the M.S. and Ph.D. degrees from the University of Southern California, Los Angeles, all in electrical engineering. He has worked as a scientist in the Defence Electronics Research Laboratory, Hyderabad, India, and as a faculty member in the Indian Institute of Technology Kharagpur and the Indian Institute of Technology Guwahati. His research interests are in diversity combining and channel modeling for wireless communications, space-time systems, cooperative communications, multiple-access systems, power line communications, molecular communications, difference equations, and linear algebra. He is a recipient of the Shanti Swarup Bhatnagar Prize, the Hari Om Ashram Prerit Dr. Vikram Sarabhai Research Award, the Khosla National Award, and the J. C. Bose Fellowship. He is a member of Eta Kappa Nu, and a fellow of IEEE, the Indian National Academies INAE, INSA, NASI, and IASc, TWAS, IET (U.K.), IETE (India), and The Institution of Engineers (India). He served as an Area Editor and an Editor for the IEEE Transactions on Wireless Communications, and as an Editor for the IEEE Transactions on Communications. He was a TPC Co-Chair for the Wireless Communications Symposium of GLOBECOM 2008 (New Orleans, Louisiana, U.S.A.) and ICC 2010 (Cape Town, South Africa), a TPC Co-Chair for the PHY Track of WCNC 2013 (Shanghai, China), and a TPC Co-Chair for the Communication Theory Symposium of ICC 2021 (online).

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Mallik is a leading researcher in the area of channel characterization and performance analysis for diversity combining systems, multiple-input multiple-output (MIMO) systems, and spacetime systems. He has made seminal contributions to performance analysis of transmit-receive diversity (use of multiple antennas at transmitter and receiver to combat effects of fading), characterization of fading channel statistics, and error analysis in correlated fading (which arises when antenna elements are closely placed). His contributions have had a substantial impact on research in wireless communications. His work is frequently cited in top quality journals, has opened significant avenues for further research.

Prof. Mallik made very significant contributions to the performance evaluation of MIMO systems. In a pioneering work, he developed a novel method for obtaining the error probability in MIMO systems as a linear combination of elementary gamma distributions. This work serves as the basis for the performance analysis of systems using MIMO technology such as 802.11n WLANs and LTE (releases 8 and 9) mobile broadband. In another pioneering work, he derived a new characterization of

a MIMO channel with number of transmitters less than number of receivers by means of the pseudo-Wishart distribution which has had a significant impact on the performance evaluation of mobile-tobase uplink communications.

In another area of significant and key contributions, Prof. Mallik took account of channel characterization by developing a general analytical framework for the multivariate Rayleigh distribution which is a very effective tool for analyzing performance in correlated Rayleigh fading. This work resulted in many useful extensions to Nakagami and other channel models which arise in mobile communication scenarios supported by Wi-Fi, EDGE, HSPA, or LTE.

Furthermore, he derived new analytical expressions for the error probability under correlated Rayleigh fading with equal-gain combining and under correlated Nakagami fading with hybrid selection/maximal-ratio combining (H-S/MRC). This seminal work is extremely useful for the design of low cost high efficiency mobile handsets, which minimize the number of RF chains at the front-end. He next analyzed the performance of a modified "minimum selection" H-S/MRC scheme that adaptively selects diversity branches based on a threshold signal-to-noise ratio, and showed its effectiveness over the usual H-S/MRC in which the number of selected branches is fixed. Its significance is that it provides a lower complexity (in terms of average number of RF chains) alternative compared to H-S/MRC, thus reducing power consumption without compromising performance. All of these works constitute important milestones in research on diversity combining schemes. He generated major results pertaining to the capacity variation of adaptive transmission systems in fading environments which have been followed by several researchers and have led to very useful extensions that greatly enhance the throughput in diverse mobile scenarios.

His significant contributions to the area of discrete-time linear systems, in which he obtained explicit solutions of linear difference equations with variable coefficients, are noteworthy. Finding such explicit solutions remained an open problem for several decades. Using novel techniques, he succeeded in solving the second, third, and Nth order cases, which constituted a significant advancement in the field.



Richa Singh Affiliation: IIT Jodhpur IEEE Fellow Citation: For contributions to robust and secure biometrics

Bio: Richa Singh received the M.S. and Ph.D. degree in computer science from West Virginia University, Morgantown, USA. She is currently a Professor with IIT Jodhpur, India and heading the Department of Computer Science and Engineering. Before joining IIT Jodhpur, she was a Professor at IIIT-Delhi. Her areas of interest are pattern recognition, machine learning, and biometrics. She has co-authored over 300 research publications in reputed venues, co-edited three books, and delivered several keynote/tutorial talks. She was a recipient of the Kusum and Mohandas Pai Faculty Research Fellowship at the IIIT-Delhi, the FAST Award by the Department of Science and Technology, India, and several best paper and best poster awards in international conferences. She is currently serving as the Program Chair of CVPR2022 and ACM ICMI 2022. She has also served as the Program Co-Chair of IJCB 2020, FG2019, and BTAS 2016, and the General Co-Chair of ISBA 2017. She is also the Vice President (Publications) of the IEEE Biometrics Council and an Associate Editor-in-Chief of Pattern Recognition. She is a Fellow of International Association of Pattern Recognition and a Senior Member of ACM.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Richa's research on unconstrained face recognition, unlike traditional research, has centered on emerging covariates such as performing face recognition when features are altered due to cosmetic plastic surgery, or when someone uses disguise or photoshop, proposing novel ways to recognize faces from 3D Kinect camera, or to be able to detect silicone mask based face spoofing when an individual uses accessories to hide their true identity or impersonate a different person, or recognizing kinship cues based on face information. To handle cross resolution face matching as in the case of surveillance videos, she led the team to propose novel paradigms such as co-transfer learning. In another work, she proposed a domain specific learning approach for newborn face recognition, an extremely challenging face recognition application of giving identity to newborns. A novel semi-supervised framework was proposed to leverage a large number of unlabeled face images to learn a suitable domain-specific representation followed by problem-specific distance metric learning. Similarly, to help investigators, often face sketches are matched against a face image gallery. To address this problem, she along with her students and collaborators proposed novel formulations, for instance, memetically optimized MCWLD. The highlight of these formulations is that they do not require large training data to optimize the performance. She also proposed an interesting forensic application of face recognition: matching skulls with face images. It is an opportunity for biometrics researchers to help the forensic experts in giving an identity to unidentified human skulls. It is an extremely challenging problem which is further exacerbated due to lack of any publicly available database related to this problem. The impact of her work can be observed by the fact that many of these research problems such as plastic surgery variations for face recognition that were introduced by her team and now, these are considered integral components of national level face recognition projects/programs.

In addition, she has made significant contributions in making pattern recognition and biometric systems robust and developed several solutions for biometric template protection and to detect attacks on face recognition systems. For instance, she developed novel algorithms to detect different kinds of physical attacks such as print attack and replay attack. Her co-authored paper received "Highest Impact Award" at CVPR Biometrics Workshop 2018. She also introduced silicone mask attack to the research community and released a database to promote research efforts in silicone mask attack. She has not only been designing algorithms to solve individual sub-problems, but looking at the overall field in a holistic manner. In practical scenarios, presentation attack detection algorithms should be robust to all the known attacks. She introduced the concept of panoptic presentation attack detection, and motivated the researchers to design algorithms that are generalizable to different attacks. She has published several papers in this area and her paper in the Senior Member Track at AAAI2020 demonstrates her expertise in this area. More recently, she has been making significant contributions in making face recognition systems robust to bias variations.



Sandeep Kumar Shukla Affiliation: IIT Kanpur/Virginia Tech IEEE Fellow Citation: For contributions to applied probablistic model checking for system design

Bio: Prof. Sandeep K. Shukla is an IEEE fellow, and ACM Distinguished Scientist. He is currently a professor of Computer Science and Engineering department at IIT Kanpur which he headed during 2017-2020. He was the editor in chief of the ACM Transactions on Embedded Computing Systems during 2013-2020. He is currently associate editors of ACM Transactions on Cyber Physical Systems, and Journal of the British Blockchain Association. In the past he has served as associate editors of IEEE Transactions on Computers, IEEE Transactions on Industrial Informatics, IEEE Design and Test, and IEEE Embedded Systems Letters. Before joining IIT Kanpur in 2015, he was a professor at Virginia Tech, USA. He served as ACM Distinguished Speaker, and IEEE Computer Society Distinguished Visitor in the past. He has authored over 200 peer reviewed journal and conference papers, and authored/edited 10 books. He was awarded the Presidential Early Career Award in Science and Engineering (PECASE) in 2004, The Bessel Award by Humboldt Foundation in 2009, a Distinguished Alumnus Award by SUNY Albany in 2007, a Ramanujan Fellowship in 2015. His major research interest is Cyber Security of Critical Infrastructures, Cyber Security of IT/OT systems, and Applications of Blockchain Technology in Security and Privacy.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Sandeep developed stochastic power management strategies for system-level power management unifying previous approaches based on Markov chain, and Markov decision procedures. This ingenious application of a probabilistic model checker used a model checker for deriving verified strategies with probabilistic guarantees, rather than as verifier. He also used model checking to derive competitive bounds on on-line dynamic power management strategies which led to a number of follow up work on using model-checkers for buffer minimization by Stujik et. Al. at DAC 2005-06. This work also inspired a thesis on game theoretic technique in high level synthesis. These were published in IEEE transactions on CAD, DATE, VLSI-D conferences among others. Sandeep also used probabilistic model checking to derive reliability-driven design of redundant logic required to guarantee a given reliability level for computations mapped onto a defective substrate – such as a self-assembled molecular fabric. While other reliability evaluation tools for digital logic was being developed in other tools such as PTM from University of Michigan, Sandeep's work showed that tensor computation involved therein are already at the core of a probabilistic model checker. Tools such as NANOLAB, and NANOPRISM were developed by Sandeep.

A large number of follow up work can be found on Google scholar in as many as 20 different groups. Much of this work appeared in multiple IEEE Transactions on CAD, on Nanotechnology, on Circuits and Systems, and multiple conferences such as DATE, IEEE-NANO, IEEE Nano-Arch, IEEE VLSI-D.

36



Sanghamitra Bandyopadhyay

Affiliation: ISI Kolkata IEEE Fellow Citation: For contributions to genetic algorithm based classification and clustering techniques

Bio: Prof. Sanghamitra Bandyopadhyay did her B Tech, M Tech and Ph.D. in Computer Science from Calcutta University, IIT Kharagpur and Indian Statistical Institute respectively. She then joined the Indian Statistical Institute as a faculty member, and became the Director in2015. Since 2020 she is continuing in her second tenure as the Director of the Institute. Herresearch interests include computational biology, soft and evolutionary computation, artificial intelligence and machine learning. She has authored/co-authored several books and numerous articles in journals, book chapters, and conference proceedings and has a citation h-index of 56. She is the recipient of several awards including the Shanti Swarup Bhatnagar Prize in Engineering Science, TWAS Prize, Infosys Prize, JC Bose Fellowship, Swarnajayanti fellowship, INAE Silver Jubilee award, INAE Woman Engineer of the Year award (academia), IIT Kharagpur Distinguished Alumni Award, Humboldt Fellowship from Germany, Senior Associateship of ICTP, Italy, young engineer/scientist awards from INSA, INAE and ISCA, and Dr. ShankerDayal Sharma Gold Medal and Institute Silver from IIT, Kharagpur, India. She is a Fellow of: INSA, National Academy of Sciences, NASI, INAE, IEEE, TWAS, International Association for Pattern Recognition (IAPR) and West Bengal Academy of Science and Technology. She was a member of the Science, Technology and Innovation Advisory Council of the Prime Minister of India (PM-STIAC) from 2018 to 2022. In March 2022, she has been conferred the Padma Shri, the fourth highest civilian award of the Government of India.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Bandyopadhyay is a world class researcher in the area of evolutionary pattern recognition where she has designed classification and clustering methods, developed their theory and studied reallife applications. In particular, her contribution in clustering, a well-known NP-hard grouping problem, is internationally acclaimed. Applications of metaheuristics like genetic algorithms (GAs) to clustering started since early-1990s. The chromosome encoding strategy adopted was point-based, with each corresponding to a data point. This severely limited the applicability of the methods to large data sets. Sanghamitra's pioneering proposal of center-based encoding strategy immediately reduced the chromosome size, speeding up convergence.

To determine the number of clusters, existing methods used an iterative approach, varying the number of clusters and estimating a measure of cluster goodness. Sanghamitra was the first to use GAs with variable length chromosomes to directly optimize novel validity indices, whose uniqueness and

global optimality for the correct number of clusters was proved. Despite all the advances, the existing methods still assumed the clusters to be convex and hyperspherical. In one stroke, Sanghamitra removed this limitation by proposing new symmetry based distance measures and concept of multiple seeds. Hence she had a technique that automatically identified the model order, was proved to converge to the partitioning with the optimal score, and identified symmetric clusters of any shape, size and overlap. Her methods are used extensively in domains like analog modulation classification, lip segmentation, biomedical and satellite image segmentation, modelling adiabatic temperature rise during concrete hydration, biometric analysis, reconstructing gene regulatory networks, identifying gene modules and detecting gene markers.

Development of AMOSA, the first effective multiobjective simulated annealing with non-greedy selection and capability of handling many objectives, is Sanghamitra's pioneering contribution in this regard. AMOSA has been used for feature selection, gene selection, microarray data clustering, finding protein modules, segmenting remote sensing images, process plan generation in reconfigurable manufacturing systems and in selection of views in data warehousing. Sanghamitra has applied her methods in computational biology, demonstrating clearly that innovative computational methods, designed by experts, are essential for making biological discoveries impacting therapeutic efforts. She developed TargetMiner, a machine learning based algorithm for predicting microRNA targets that provided the best specificity-sensitivity trade-off because of its systematic identification of tissue specific negative samples. Genome-wide TargetMiner predictions are indexed by miRBase, a heavily used microRNA repository. Building upon these predictions, Sanghamitra revealed miR-155 as a genetic marker for breast cancer.



Sankar Kumar Pal

Affiliation: ISI Kolkata IEEE Fellow Citation: For contributions to pattern recogntlon and image processing using Fuzzy set theoretic methods

Bio: Sankar K. Pal received PhD degrees from the University of Calcutta, Kolkata, and Imperial College, London. He joined the Indian Statistical Institute, Kolkata in 1975 as a CSIR-SRF where he became a full professor in 1987, a distinguished scientist in 1998, and the Director in 2005. Currently, he is a National Science Chair, and ISI-Emeritus Professor. He founded the Machine Intelligence Unit and the Center for Soft Computing Research at his Institute in Kolkata. He is a former INSA Distinguished Professor, INAE Chair Professor, Jawaharlal Nehru Fellow, and J.C. Bose National Fellow.He worked at the University of California, Berkeley, CA, USA; University of Maryland, College Park, MD, USA; NASA Johnson Space Center, Houston, TX, USA; and US Naval Research Laboratory, Washington, DC, USA. He held several visiting positions in Italy, Poland, Hong Kong, and Australia. He has coauthored 21 books and over 450 research publications in the areas of pattern recognition, machine learning, image/video processing, data mining, web intelligence, soft computing, bioinformatics, social-network analysis, and cognitive machines.

Prof. Pal received several national/ international awards including the S.S. Bhatnagar Prize, the Padma Shri, G.D Birla Award, Om Bhasin award, Khwarizmi International Award (Iran), and NASA Tech Brief (USA). He is an IEEE-Computer Science Distinguished visitor since 1987. He is/was on the editorial boards of 25 journals including several IEEE Transactions. He has visited 45 countries as a keynote/ invited speaker and academic visitor. He is a Fellow of TWAS, IAPR, IFSA, and all four National Academies for Science/Engineering in India.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Sankar K. Pal (Fellow'1993-LifeFellow'2015) has made fundamental contributions to machine intelligence research by developing various modern approaches. He pioneered the development of fuzzy set theory and neuro-fuzzy computing, in general, and their applications in pattern recognition and image processing, in particular. For example, his work on fuzzy image processing (IEEE-T-SMC-11, 494-501, 1981; IEEE-T-PAMI-4, 204-208,1982; IEEE-T-PAMI-5, 69-77, 1983; IEEE-T-SMC-13, 94-100, 1983) is perhaps the first investigation (other pioneer was Azriel Rosenfeld, UMD, College Park) that brings out the root relation between the abstract concept of fuzzy sets and image processing tasks. Here, a gray-tone image is defined as an array of fuzzy singletons representing the degree of possessing some image property or belonging to some ill-defined image subsets, like region, boundary and edge which do not lend themselves to precise definition. It was shown how the ambiguity measure, like "index of fuzziness" or "entropy" reduces with image-contrast enhancement corresponding to different shapes/slopes of an S-type membership function. Again, by

changing the cross-over point of the S-function over the grayscale and computing the image-ambiguity, one can determine the optimum threshold level(s) and fuzzy image segmentation(s) for which the said ambiguity measure attains minima (Pattern Recog. Letters, 1, 141-146, 1983). This basic model, viz, image definition and use of fuzziness measures for modelling ambiguity and optimum-object extraction, has laid the foundation of the fuzzy image processing research. A definition of image entropy using logarithmic/exponential gain functions is provided (IEE-Proceedings-E, 136, 284-295, 1989).

40



Shanthi Pavan Affiliation: IIT Madras IEEE Fellow Citation: For contributions to delta-sigma data converters and analog filters

Bio: Shanthi Pavan obtained the B. Tech degree from the Indian Institute of Technology, Madras in 1995 and the M.S and Sc.D degrees from Columbia University, New York in 1997 and 1999 respectively. He is now with the Indian Institute of Technology-Madras, where he is now the NT Alexander Institute Chair Professor of Electrical Engineering. His research interests are in the areas of high speed analog circuit design and signal processing.

Dr.Pavan is the recipient of several awards, including the IEEE Circuits and Systems Society Darlington Best Paper Award (2009), the Shanti Swarup Bhatnagar Award (2012) and the Swarnajayanthi Fellowship (2009) (from the Government of India). He is the author of Understanding Delta-Sigma Data Converters (second edition), with (Richard Schreier and Gabor Temes), which received the Wiley-IEEE Press Professional Book Award for the year 2020.Dr.Pavan has served as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems: Part I - Regular Papers on the technical program committee of the International Solid State Circuits Conference, and been a Distinguished Lecturer of the Solid-State Circuits and Circuits-and-Systems Societies. He currently serves as the Vice President of Publications for the IEEE Solid-State Circuits Society, and on the editorial boards of the IEEE Journal of Solid-State Circuits and the IEEE Solid-State Circuits Letters. He is a fellow of the Indian National Academy of Engineering, and an IEEE fellow.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Pavan's contributions have spanned the areas of data converters and filter design. The salient aspects of his work in these areas are the following:

(a) Development of design techniques for delta-sigma data converters, and demonstration of several state-of-the-art designs incorporating these techniques. Of particular importance is demystifying and demonstrating the use of FIR feedback in continuous-time delta-sigma converters. Many of these techniques have been incorporated in industrial products by companies across the globe.

(b) Co-authoring the book : Understanding Delta-Sigma Data Converters (2nd Edition) with R.Schreier and G.Temes, which has been adopted in multiple schools worldwide.(c) Development of design techniques for active analog filters, from low- to microwave frequencies, for applications ranging from radios to serial communication.



Shrikrishna V. Kulkarni

IIT Bombay IEEE Fellow Citation: For contributions to transformer engineering education

Bio: Dr. S. V. Kulkarni is Institute Chair Professor in the Department of Electrical Engineering and Dean (Administrative Affairs) at IIT Bombay. He was INAE (Indian National Academy of Engineering) Chair Professor in the Department during April 2018 - March 2020. He is a Fellow of IEEE & INAE and IEEE PES Distinguished Lecturer. He was Editor of IEEE Transactions on Power Delivery and IEEE Power Engineering Letters (2012-2019). He worked at Crompton Greaves Limited (1990-2001) and specialized in the design and development of transformers up to 400 kV class. He was a recipient of the Young Engineer Award conferred by INAE in 2000 for his contributions to 'Electromagnetic Field Computations and High Voltage Insulation Design in Transformers'. He was also honoured with the Career Award for Young Teachers from AICTE in 2001. He received Best Paper Awards in international conferences on transformers held in 2002 and 2006. He has authored a book Transformer Engineering: Design, Technology, and Diagnostics, Second Edition, published by CRC Press in September 2012 and he received IIT Bombay Research Dissemination Award 2016. He has also written a chapter 'Challenges and Strategies in Transformer Design' in the book 'Transformers: Analysis, Design, and Measurement' published by CRC. He has adapted an undergraduate text book on electromagnetics for Asia, Principles of Electromagnetics, Oxford University Press, published in October 2015. He has set up the Field Computation Laboratory and the Insulation Diagnostics Laboratory in the Electrical Engineering Department at IIT Bombay. He has 200 publications two US patents. For more details see: http://www.ee.iitb.ac.in/wiki/faculty:svk

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Shrikrishna V. Kulkarni has made distinctive and lasting contributions as an outstanding educator in the area of transformers. His book, Transformer Engineering: Design, Technology and Diagnostics, CRC Press, comprehensively deals with the design, performance, operation, diagnostics, and system interaction aspects. The relevant theory of electromagnetic fields and Finite Element Method has been covered in depth, which is the most striking feature of the book. The value of the book is in its nice blend of theory and practice throughout the text. This is because of his previous rich industrial experience of 11 years at a power transformer manufacturer (1990-2001), and his current academic/research experience since 2001. The book's global acceptance is evident in the fact that its version in the Chinese language has been published in 2016 by China Machine Press. He received an award from his Institute for outstanding efforts in disseminating research through the book. Realizing the depth and breadth of Prof. Kulkarni's knowledge, the Global R&D Manager of ABB Power Transformers invited him in 2010 and 2012 to give lectures at the ABB Corporate Research Center in

Vasteras, Sweden. He has given invited talks and tutorials in Workshops on Transformers held in Spain (2019, 2010, 2007, 2004), Croatia (2014), and Mexico (2004). The book has been cited more than 1200 times by researchers as evident in Google Scholar and is also used as a reference in courses in different universities. He has published 84 articles in reputed journals (28 in IEEE Transactions). His publications have been cited more than 3500 times (Source: Google Scholar). Prof. Kulkarni has been significantly contributing to IEEE activities. He was Editor of IEEE Transactions on Power Delivery (2012-2019). He was Co-Chair of IEEE-INAE (Indian National Academy of Engineering) Symposium on Electromagnetic Education and Research (2016). He was Education Activities Chair in 2019-2020 and PES-IAS Joint Chapter Chair in 2021 of IEEE Bombay Section. He is currently Vice Chair Awards IEEE India Council since 2021.

His other significant contribution is in the area of educating engineering community on electromagnetics. Looking at his expertise in electromagnetics, he was invited to adapt an undergraduate text book 'Principles of Electromagnetics' for Asia. He has set up a Virtual Electromagnetics Laboratory (https://www.ee.iitb.ac.in/course/~vel/) which has been visited by more than 24000 visitors till now. Prof. Kulkarni is known for his leadership in education and research in India, and he was selected as a Fellow of Indian National Academy of Engineering with effect from 2012. Currently, he is a member of Academy's Sectional Committee on Electrical Engineering, which is responsible for recommending names of Fellows to be selected every year. He has contributed at the national level as a member of committees which advise Government of India on R&D policy matters. He was Chairman of committees of Ministry of Science and Technology and Ministry of Power, for shortlisting and recommending research projects for funding. He has conducted 20 training programs (each of 2 to 5 days) for industries and academia in India on Power Transformers and Computational Electromagnetics. He has also organized a workshop on 'Electromagnetics: Pedagogy and Research Trends' for faculty members of academic institutes in India. He has also given more than 60 guest lectures at various engineering colleges in India on electromagnetics and transformer engineering. He has completed 7 research projects funded by Indian Government and industries. He has also provided consultancy through 25 projects to transformer and other industries in India.



Soumitro Banerjee Affiliation: IISER Kolkata

IEEE Fellow Citation: For contributions to the understanding of nonlinear phenomena in power electronic circuits, and to the theory of border collision bifurcation

Bio:Dr. Soumitro Banerjee (born 1960) did his B.E. from the Bengal Engineering College (Calcutta University) in 1981, M.Tech. from IIT Delhi in 1983, and Ph.D. from the same Institute in 1987. He was in the faculty of the Indian Institute of Technology, Kharagpur, since 1986, and has moved to the Indian Institute of Science Education & Research, Kolkata, in 2009.

Dr. Banerjee's areas of interest are the nonlinear dynamics of power electronic circuits and systems, and bifurcation theory for nonsmooth systems. He has published four books: "Nonlinear Phenomena in Power Electronics" (Ed: Banerjee and Verghese, IEEE Press, 2001), "Dynamics for Engineers" (Wiley, London, 2005), "Wind Electrical Systems" (Oxford University Press, New Delhi, 2005), and "Research Methodology in Natural Sciences" (IISc Press, 2022). Dr. Banerjee served as Associate Editor of the IEEE Transactions on Circuits & Systems II(2003-05), and as Associate Editor of the IEEE Transactions on Circuits & Systems I (2006-2007). He is a recipient of the S. S. Bhatnagar Prize (2003), and was recognized as a "Highly Cited Author" by Thomson Reuters from 2004 to 2014. He is a Fellow of the Indian Academy of Sciences, the Indian National Academy of Engineering, the Indian National Science Academy, The World Academy of Sciences, and the IEEE.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Scientists studying changes taking place in the material world have found that the changes can be quantitative as well as qualitative. Such qualitative changes are found both in its state of existence (like ice turning into water), and in its state of motion (like a regular periodic behaviour changing into an aperiodic and unpredictable one). The qualitative changes in the state of motion are called bifurcations --- which have been the subject of investigation of Dr. Banerjee.

He has studied these bifurcation phenomena in a particular class of dynamical system which involve some kind of switching action that makes the system toggle between two or more different types of dynamical behaviour. Common examples of such "hybrid systems" are the power electronic circuits, mechanical systems where impacts between bodies take place (like walking robots), the human heart, etc. Dr. Banerjee has shown that such systems undergo a special kind of qualitative change, known as "border collision bifurcation." Hehas been instrumental in developing the theory of border-collision bifurcations, which hasbeen widely used in application areas to understand why certain abrupt and drastic changes occur in the dynamical state of a system when a parameter is smoothly varied. He has also been in the forefront in the investigations on the nonlinear phenomena in power electronics.



Sri Niwas Singh Affiliation: ABV-IIITM Gwalior/IIT Kanpur IEEE Fellow Citation: For leadership and contributions to power engineering education

Bio: Prof S. N. Singh obtained his M. Tech. and Ph. D. in Electrical Engineering from IIT Kanpur, in 1989 and 1995 respectively. Presently, Prof Singh is Director, ABV-IIITM Gwalior(on leave from Professor (HAG), IIT Kanpur). Before joining IIT Kanpur, Dr Singh worked with UP State Electricity Board from 1988 to 1996, IIT Roorkee from 1996 to 2000 and with Asian Institute of Technology, Bangkok from 2001 to 2002. He was Vice-Chancellor of Madan Mohan Malviya University of Technology Gorakhpur during April 2017 to July 2020.

Prof. Singh received several awards including Young Engineer Award of INAE, Khosla Research Award of IIT Roorkee, and Young Engineer Award of CBIP New Delhi. Prof Singh is receipt of Humboldt Fellowship of Germany (2005, 2007) and Otto-monsted Fellowship of Denmark (2009-10). Prof Singh became first Asian to receive 2013 IEEE Educational Activity Board Meritorious Achievement Award in Continuing Education. He is also recipients of INAE Outstanding Teacher Award and IEEE R10 Outstanding Volunteer Award 2016. Dr Singh is appointed as IEEE Distinguish Lecturer of Power & Energy Society from 2019 and Industry application Society for 2019-2021. He is also recipient of NPSC 2020 Academic Excellence Award and 2021 IEEE Industry Application Society Outstanding Educator/ Mentor Award.Prof Singh has supervised 40 PhD (8 under progress). Prof Singh was Chairman, IEEE UP Section for 2013 & 2014, IEEE R10 (Asia-Pacific) Conference & Technical Seminar Coordinator 2015-18 and R10 Vice-Chair, Technical Activities (2019-2020). Presently Prof Singh is Immediate Past Chairman of IEEE India Council. Prof Singh is Fellows of IEEE, IET, INAE, IE(I), IETE, and AvH.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. S. N. Singh has contributed to the power system profession in several roles: as a meritorious student (10.0/10.0 CPI), as a competent utility engineer (first 800 kV transmission system design study), as a world-class researcher (500+ published research papers) and as an outstanding educator (accolades from Chairman, Senate of IIT Kanpur). From 1988 to 1995, Dr. Singh was simulation experts who did transmission system planning for the Uttar Pradesh State Electricity Board. He was instrumental in the study of the first 800kV transmission system (Anpara-Unnao line) design in India. From 1995 to 1996, he managed the operation and control of Obra thermal power plant (2x200 MW). Due to inclination of engineering education and research, Prof Singh switched to academics in 1996. Since then, he has been a faculty/researcher in several prestigious universities such as AIT Bangkok, DTU Denmark, University of Duisburg-Essen Germany, Hong Kong PolyU, IIT Roorkee and IIT

Kanpur. Prof. Singh is passionate about improving the quality of electrical engineering education and research. This can be seen from his persistent efforts and contributions toward screating a strong workforce through continuing education programs/ e-learninginitiatives/ technology enhanced learning schemes. He has written two popular undergraduate books on fundamentals of power system, of which more than 25000 copies have been sold. He has also written six book chapters on advanced topics in power systems and developed two video courses on Power System Operation and Control, and HVDC Transmission (about 38 one hour lectures for each) under a Government of India initiative. The quality and popularity of his teaching can be gauged by looking at the number of total views of his online lectures (> 440,000) which are also available on YouTube (> 89k hits).

In 2002, Dr. Singh designed and developed a postgraduate course on Electricity Markets at IIT Kanpur which was the first of its kind in any Indian Institute/ University. His research is streamlined on modern electric grid with emphasis on electricity markets, artificial intelligence, flexible AC transmission systems, renewable energy integration and power quality issues. He has published more than 500 research papers in peer-reviewed journals and conference proceedings. Total citation to his work being more than 12000 and H-index of 57. He has already mentored 67 postgraduate students with 10 current postgraduate students. The research of Dr. Singh in the area of industrial-electronics applications in the power systems has been world class and has immensely influenced number of power system researchers and professionals acorss globe. He has successfully executed several research oriented projects in India and abroad. A Real Time Digital Simulation(RTDS) facility (six racks), the biggest facility in any academic institute in Asia, was set up at IIT Kanpur by the active support of Dr Singh. This facility is being tremendously utilized by Indian industries and academic institutions for the advance and practical research. He was asked to develop a special course module on "Distribution Equipments: Technology and Applications" by Power Finance Corporation under the Ministry of Power for the upgrading the skills of the utilities personnel. This program was well appreciated by Level-B engineers.



Srinivasan Ramani Affiliation: IIIT Bangalore IEEE Fellow Citation: For contributions to computer networks for developing countries

Bio: Srinivasan Ramani proposed an Indian Academic Network in 1983, and this contributed to the launch of the Education and Research Network project of the Government of India, involving several institutions. As coordinator of the ERNET team at India's National Center for Software Technology (NCST), he led the efforts to set up ERNET's central mail switch and its international gateway with a link to Amsterdam in 1987 using TCP over X.25. This was the first international connection to the Internet from India. A year later, his team connected ERNET to UUNET in the US. Partnering institutions of ERNET, cooperating with Ramani's team at NCST, set up domestic TCP/IP links extending the network nation-wide.Earlier, Ramani's team had created communication software for the Indian-made TDC-316 in 1976-77, using it for education. He played a key role in creating an experimental satellite-based packet switching network in 1981 and co-authored a pioneering paper proposing a Low Altitude Equatorial Satellite for computer messaging in 1982. Others built such a satellite and demonstrated its utility internationally.

Srinivasan Ramani was inducted into the Internet Society's Hall of Fame in 2014. He has served as founding director of the National Centre for Software Technology, first director of Hewlett Packard Labs India, and professor at International Institute of Information Technology, Bangalore. He is a Fellow of the IEEE, Computer Society of India, and Indian National Academy of Engineering and has served as a member of the Expert Panel of Advisors of the UN Task Force on ICT for Development.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Srinivasan Ramani has contributed significantly to the cause of bringing the benefits of network technology and its applications to India and has also promoted other developing countries to adopt this technology. He has been working in this area since mid-seventies and has played key roles in a project that created the academic network of India. Ramani has led R & D activities and has educated over a thousand students at the post-graduate level. He has played a notable role in taking Internet technology to the financial services sector. He recognized early on that online education would be a very significant application of the Internet and has championed the cause of technology for education in India in addition to doing significant R & D in this area.

ERNET: Please see the text describing this work in the biographical note.

Work on Computer Communication for Developing Countries:He started a series of conferences named Computer Communication for Developing Countries in 1987 and ran it for many years, holding events in many developing countries in Asia and Africa.

47

Education in the areas of Networks and Software Technology: Dr. Ramani was given the mandate by the Government of India to set up a research and education institution in 1984-85. He played a key role in conceptualizing the National Centre for Software Technology (NCST). Much of Dr Ramani's later research emanated from NCST, while it became one of the best educators of world-class software professionals in the country. He served as the first director of NCST, during 1984-2000, after playing a key role in founding the institution.Ramani has taught courses in computer networks and software technology to over a thousand post-graduate students, creating trained human resources in this area at a critical period when India was adopting Internet technology in a big way.

Work on Applications of Internet Technology in India:Dr Ramani's engagement with networking helped many institutions build their own networks – the earliest amongst them being the network for Press Trust of India (PTI). He also designed nation-wide WANs for many major banks, stock exchanges and oil companies in India. He was a consultant during 1997-99 in planning the technical infrastructure for MTNL's ISP venture. Dr. Ramani's work has had major impact on academic institutions, financial institutions, government, and the IT industry.

Work inside IEEE:Ramani was the Indian Coordinator on the IEEE CS Chapter Activities Board during 2007-08 and played a key role in creating the IEEE Computer Society's Bangalore Chapter; earlier there had been a single common IEEE Society Chapter for Communications, Computers and Management.



Surendra Pal Affiliation: Ex-TIFR, ISRO, DRDO, DIAT

IEEE Fellow Citation : For advancing space and RF communication technology in India, since the inception of Indian Space Programme including Satellite Navigation Activities(GAGAN and NavIC)

Bio: Fellow of: IEEE, NAE, NASc, Dist. Fellow ASI, IETE, VEDA, IET(UK)ATMS(I),

Chartered Engineer (UK), Distinguished Alumini BITS - Pilani

FORMER:Vice -Chancellor Defence Institute of Advanced Technology Pune,Prof.DS Kothari DRDO Chair(2018-2020).Dhawan Professor & Senior Adviser SATNAV - ISRO,Distinguished Scientist and Founding Programme Director Satellite Navigation-URSC(ISAC) ISRO Bangalore.RF & GNSS Consultant,Distingushed Visiting Professor INAE-India,Distinguished Lecturer-IEEE(AES-Society),Hon.Professor-Amity University (UP) and Techno India University (WB) ,Chairman GAGAN(A joint ,satellite based GPS wide area augumentation system -GAGAN, of ISRO and AAI),Associate Director ISAC(URSC)-ISRO,Member AICTE Governing Council(2012-14),President IETE(2012-2014),Senior Adviser and Consultant-Centre for Internet and Society -Bangalore,Senior Adviser -ICT-Ahmedabad University,Aditya Birla Chair -BKBIT Pilani,ITU Consultant,ICO Consultant and GNSS Expert for UN Office for Outer Space.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

For advancing space and RF communication technology in India, since the inception of Indian Space Programme including Satellite Navigation Activities (GAGAN and NavIC). Expertise in Electromagnetics, Antennas, Microwave-Communication-circuit and system designs, Space communication, Radars, Digital Communication particularly high bit rate data transmission from space and initiating and advancing Satellite Navigation Activities in India.



Sushil Kumar Soonee Affiliation: POSOCO Alumni IEEE Fellow Citation: For leadership in developing operational methods for power grid interconnection in India

Bio: Former Advisor POSOCO, Former and Founder Chief Executive Officer, Power System Operation Corporation Ltd. S K Soonee is a Life Fellow of Institution of Engineers (India), Fellow IEEE, Distinguished Alumnus IIT Kharagpur, Distinguished Member CIGRE, Fellow INAE, International Member NAE, USA.

https://www.researchgate.net/profile/Sushil-Soonee/research

https://www.linkedin.com/in/soonee/

https://twitter.com/sksoonee

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Soonee has first-hand four decades of experience of Power System Operation of various Regional Grids of India and has worked extensively towards Integration of Grids leading to the formation of the National Grid and now SAARC Grid.

Soonee specializes in Power System Operation, Planning, Commercial, Settlement, Restoration and entire gamut of Power Pooling and Governance. Other areas of interest include Electricity Markets, Open Access, Regulatory affairs besides expertise in Load Despatch Technology, integration of Renewable Energy including REC Mechanism, Transmission Pricing and development of Ancillary Services. Soonee has represented India on the CIGRE Study Committee C2 on Power System Operation and the CIGRE Study Committee C5 on Electricity Markets and Regulation.



Sushmita Mitra Affiliation : ISI Kolkata IEEE Fellow Citation: For contributions to neuro-fuzzy and hybrid approaches in pattern recognition

Bio: Sushmita Mitra is a full professor at the Machine Intelligence Unit, Indian Statistical Institute, Kolkata. From 1992 to 1994 she was in the RWTH, Germany as a DAAD Fellow. She was a Visiting Professor in the University of Alberta, Canada; Meiji University, Japan; and Aalborg University, Denmark. Dr. Mitra received the National Talent Search Scholarship (1978-1983) from NCERT, the University Gold Medal in 1988, the IEEE TNN Outstanding Paper Award in 1994 for her pioneering work in neuro-fuzzy computing, the CIMPA-INRIA-UNESCO Fellowship in 1996, and Fulbright-Nehru Senior Research Fellowship in 2018-2020. She was the INAE Chair Professor during 2018-2020, J. C. Bose National Fellowship, 2021.

Dr. Mitra is a Fellow of: IEEE, TWAS, INSA, INAE, NASc, International Association for Pattern Recognition. She is an IEEE CIS Distinguished Lecturer, Member of Inter-Academy Panel Panel for Women in STEMM, and the current Chair, IEEE Kolkata Section. Her current research interests include data science, pattern recognition, soft computing, medical image processing, and Bioinformatics. Dr. Mitra is ranked among the top 2% scientists worldwide in the domain of Artificial Intelligence and Image Processing.Dr. Mitra is the author of the books: ``Neuro-Fuzzy Pattern Recognition: Methods in Soft Computing', ``Data Mining: Multimedia, Soft Computing, and Bioinformatics'' and ``Introduction to Machine Learning and Bioinformatics'', beside a host of other edited books. Dr. Mitra, is an Associate Editor of ``IEEE/ACM Trans. on Computational Biology and Bioinformatics'', ``Information Sciences'', ``Fundamenta Informatica'', ``Computers in Biology and Medicine'', SN Computer Sciences and is a Founding Associate Editor of ``Wiley Interdisciplinary Reviews: Data Mining and Knowledge Discovery''. She has more than 150 research publications in referred international journals.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Dr. Sushmita Mitra has made outstanding contributions in pattern recognition and machine intelligence, synergistically, at theoretical and application levels. She has pioneered a generic family of hybrid approaches for data mining, integrating fuzzy and rough sets with neural networks and decision trees. Her seminal contribution lies in neuro-fuzzy rule generation, particularly for the extraction of classificatory linguistic rules from fuzzy neural networks, thereby promoting their understandability. This encompassed inferencing for unknown test cases, querying in the presence of incomplete/missing information, and justification for an inferred decision. This led to the development of neuro-fuzzy expert systems, culminating in the IEEE-NNC Outstanding Paper Award in 1994, with two of her

papers ranking in the list of Top-cited papers in Engineering from India. The unique idea of exploiting rough sets, for knowledge encoding, enhanced the power of computational models in terms of learning, performance, speed, understandability and compactness. This provides the basic module for subsequent hybrid-rough research in pattern recognition. Shadowed clustering has been introduced by Dr. Mitra as a conceptual and algorithmic bridge between fuzzy and rough clustering, thereby robustly and efficiently incorporating the generic merits of both. A rough-fuzzy collaborative clustering architecture has been developed for the parallel discovery of a common global structure in a distributed framework involving large data. This has application in agent-based systems. Such hybridization has been successfully employed in correctly segmenting CT scan images of the brain, under various kinds of infarction, in the presence of ambiguity. Automated staging of cervical cancer, along with the generation of diagnostic rules, has been designed for early prognosis and treatment of cancer.

She designed new methodologies for mining high-dimensional gene expression data, to extract gene interaction pathways, with applications to cancer research. A multi-objective evolutionary-rough framework selects a small subset of necessary genes, while efficiently handling the conflicting criteria of enhanced performance under reduced cardinality. Biclustering genes, in such multi-objective framework, helped detect coherent subsets of genes responsible for cancerous conditions in microarray data. A new curve-fitting approach was designed, based on minimization of least-squares error between gene pairs along with higher-order dependencies. This patented concept has been employed to extract gene regulatory subnetworks from time series gene expression data, while eliminating the need for user-defined parameters. A novel deep learning system was developed for effective, automated segmentation of different sub-regions viz. edema, necrosis, enhancing and non-enhancing tumor core, from multi-modal MR images of the brain. Concepts of spatial-pooling and unpooling were used to preserve the spatial locations of the edge pixels, for reducing segmentation error around the boundaries. An encoder-decoder type convolutional network was designed for pixel-wise segmentation of the tumor along three anatomical planes (axial, sagittal, and coronal) at the slice level. These were then combined, by incorporating a consensus fusion strategy with a fully connected Conditional Random Field based post-refinement, to produce the final volumetric segmentation of the tumor and its constituent sub-regions. Introduction of ensembling into the deep learning framework enabled enhanced segmentation of brain tumor sub-regions in 3D, along with improved patient survival prediction. The model was ranked among the top four methods, by the leaderboard score, in the MICCAI 2019 Challenge.

52



Ujjwal Maulik Affiliation: Jadavpur University IEEE Fellow Citation: For development of algorithms in evolutionary clustering and bioinformatics

Bio: Dr. Ujjwal Maulik is a Professor in the Dept. of Comp. Sc. and Engg., Jadavpur University since 2004. He was also the former Head of the same Department. He also held the position of the Principal in charge and the Head of the Dept. of Comp. Sc. and Engg., Kalayni Govt. Engg. College. Dr. Maulik has worked in many universities and research laboratories around the world as visiting Professor/ Scientist including Los Alamos National Lab., USA, Univ. of New South Wales, Australia, Univ. of Texas at Arlington, USA, Univ. of Maryland at Baltimore County, USA, Fraunhofer Institute for Autonome Intelligent Systems, St. Augustin, Germany, Tsinghua Univ., China, Sapienza Univ., Rome, Italy, Univ. of Heidelberg, Germany, German Cancer Research Center (DKFZ), Germany, Grenoble INP, France, University of Warsaw, University of Padova, Italy, Corvinus University, Budapest, Hungary, University of Ljubljana, Slovenia, International Center for Theoretical Physics (ICTP), Trieste, Italy in.

He is the recipient of Alexander von Humboldt Fellowship during 2010, 2011 and 2012 and Senior Associate of ICTP, Italy during 2012-2018. He is the Fellow of: INAE, NASI, International Association for Pattern Recognition (IAPR), USA and IEEE. He is also the Distinguish Member of the ACM. He is Distinguish Speaker of IEEE and ACM. His research interest include Machine Learning, Pattern Analysis, Data Science, Bioinformatics, Multi-objective Optimization, Social Networking, IoT and Autonomous Car. In these areas he has published ten books, more than four hundred papers, mentoring several start-ups, filed several patents and already guided twenty two doctoral students.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Contribution in Evolutionary Clustering, Multi-Objective clustering, developing cluster validity index as well developing algorithms for biological data.



V K Atre Affiliation : Ex-DDR&D/DRDO IEEE Fellow Citation: For expertise in signal processing and underwater technology

Bio: Obtained Ph.d from Universityo of waterloo, canada. Taught at technical university of Nova Scotia. Joined Defence R&D in India at Naval Research lab. Became the Director General of Defence R&D and Scientific Advisor to Defence Minister, Govt of India. Awaraded Padam Bhushana and Padma Vibushana Civilian awards from Government of India. Started MEMs and Microsystems research in India.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

For Defence Underwater Technology and Development of Sonar suites for all the three dimensions of Navy. Guiding development of Electrornic warfare Systems for defence services. Providing technology leadership in developing defence technologies.



V Ramgopal Rao Affiliation : IIT Delhi IEEE Fellow Citation : For contributions to CMOS System-on-Chip technologies

Bio: Prof. V. Ramgopal Rao is currently a Professor in EE and the immediate Past Director of IIT Delhi. Before joining IIT Delhi as the Director in April 2016, Dr. Rao served as a P. K. Kelkar Chair Professor for Nanotechnology in the Department of Electrical Engineering. Dr. Rao has over 480 research publications in the area of nano-scale devices & Nanoelectronics and is an inventor on 49 patents and patent applications, which include 18 issued US patents. Thirteen of his patents have been licensed to industries for commercialization. Prof. Rao is a co-founder of two deep technology startups at IIT Bombay (Nanosniff&Soilsens) which are developing products of relevance to the society. Dr. Rao is a Fellow of: IEEE, INAE, INSA, NASI, IASc.

Prof. Rao's research and leadership contributions have been recognized with over 35 awards and honors in the country and abroad. He is a recipient of three honorary doctorates. The recognitions Prof. Rao received include the Shanti Swarup Bhatnagar Prize in Engineering Sciences, Infosys Prize, IEEE EDS Education Award, Excellence in Research awards from IIT Bombay, DAE and DRDO, Swarnajayanti Fellowship award from the Department of Science & Technology, IBM Faculty award, Best Research award from the Intel Asia Academic Forum, Techno-Visionary award from the Indian Semiconductor Association, J.C.Bose National Fellowship among many others. Prof. Rao was an Editor for the IEEE Transactions on Electron Devices during 2003-2012 for the CMOS Devices and Technology area and currently serves on the Editorial Advisory Board of ACS Nano Letters, a leading international journal in the area of Nanotechnology. He also serves as an Editor for the IEEE Journal on Flexible Electronics.

Dr. Rao served as the Chairman, IEEE AP/ED Bombay Chapter and as a Vice-Chairman, IEEE Asia Pacific Regions/Chapters sub-committee for two terms. He was the first elected Chairman for the India section, American Nano Society during 2013-2015.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Prof. Rao has made significant contributions to the high-voltage drain extended (DEMOS) devices and their failure mechanisms for System-on-Chip (SoC) applications. Specifically, in a series of seven publications in IEDM & IRPS and through six US patents filed jointly with semiconductor industries, he has proposed robust drain extended MOS devices, novel ways of introducing high voltage handling capabilities in FinFETtechnologies, an IGBT device with plugged-in SCR for robust ESD protection in FinFET technologies and demonstrated a dual gate STI DEMOS with improved mixed-signal and hotcarrier reliability. Working jointly with Infineon and later with Intel, he has developed a single halo DEMOS for robust ESD protection in advanced high voltage CMOS and realized a DEMOS device using a dual STI process. The modified DeMOS devices were found to be highly reliable under the ESD conditions in addition to exhibiting an excellent mixed signal performance. Based on the physical understanding provided by his work, the engineered or newly invented DeMOS devices realized in Infineon were found to be highly reliable with a 2X higher performance improvement, which is a breakthrough in the field of microelectronics.



Venkata Padmanabhan

Affiliation: Microsoft Research India IEEE Fellow Citation: For contributions to networked and mobile computing systems.

Bio: Venkat Padmanabhan (https://research.microsoft.com/~padmanab/) is Deputy Managing Director at Microsoft Research India in Bengaluru. He was previously with Microsoft Research Redmond, USA for nearly a decade. Venkat's research interests are broadly in networked and mobile systems, and his work over the years has led to highly cited papers, technology transfers within Microsoft, and also industry impact. He received the Shanti Swarup Bhatnagar Prize in 2016 and test-of-time awards from SIGMOBILE (2016 & 2019), SenSys (2019), and SIGMM (2020). He was also among those recognized with the SIGCOMM Networking Systems Award 2020, for contributions to the ns family of network simulators. Venkat holds a B.Tech. from IIT Delhi (from where he received the Distinguished Alumnus award in 2018) and an M.S. and a Ph.D. from UC Berkeley, all in Computer Science, and has been elected a Fellow of the INAE, the IEEE, and the ACM. He is an adjunct professor at the Indian Institute of Science and was previously an affiliate faculty member at the University of Washington.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

1. Persistent connections and pipelining to significantly improve HTTP performance. Incorporated in the HTTP/1.1 Internet standard.

2. Other work on improving web latency, including predictive prefetching and TCP fast start.

3. The RADAR system for indoor localization using RF-based wireless LANs and follow-on work on EZ to eliminate the need for calibration.

4. IP2Geo work on geolocation of Internet hosts based just on their IP address.

5. Other contributions to wireless networking (TCP performance, multi-hop capacity), peer-to-peer streaming, and green computing.



Viswanadham Nukala Affiliation: Ex-IISc Bangalore IEEE Fellow Citation : For contributions to the modelling and performance analysis of Flexible manufacturing systems

Bio: N. Viswanadham is INSA Honorary Scientist in the Computer Science and Automation at the Indian Institute of Science. From 1967-98, he was faculty at the Indian Institute of Science (IISc). Professor Viswanadham was Professor and Executive Director for The Center of Excellence Global logistics and manufacturing strategies at ISB during 2006-2011. He was Deputy Executive Director of The Logistics Institute-Asia Pacific and Professor at the National University of Singapore during 1998-2005.

Professor Viswanadham has several research distinctions. He was a GE Research Fellow during 1989-90, Tata Chemicals Chair Professor at the Indian Institute of Science, Bangalore, and the recipient of the 1996 IISc Alumni award for excellence in research. He also won the IBM faculty award in 2006 and was conferred the Distinguished Alumni Award for the year 2009 by the Council of the Indian Institute of Science. He received 2012 INAE Prof S K Mitra Memorial Award.Professor Viswanadham has made significant contributions to the areas of manufacturing, logistics and global supply chain networks. He is the author of Four Textbooks, Nine Edited Volumes, over two hundred forty journal and top tier conference papers. His current research efforts are on use of New Technologies for Future Supply chain network design using blockchains and smart contracts, Design of Competitive Business Models and Application to Healthcare and Agriculture supply chains. He has done academic and industry relevant research all through his career and has interacted with industrialists in India and abroad. Currently he acts as a knowledge-based NGO advising lot of start-ups.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Professor ViswanadhamJoined IEEE in 1987 as senior member, was elected as fellow 1993 and became a life fellow in 2014. His research areas were Control systems, large scale systems during the sixties. I shifted to computer control systems during seventies concentrating continuous process control systems. We also worked on design of reliable computer control systems.Professor Viswanadhamstarted working on manufacturing systems in the 80's, Supply chain automation in the 90, s, During the late 70,s and early 80's Factory floor automation was the key issue. Integrated manufacturing factory floors using numerically control machines, Robots for transfer of material, automated guided vehicles were being designed and built by auto and other industry giants such as GE. Local area network protocols were used to interconnect the PLCs. He was working on design of factory control systems using analytical techniques. These were called Flexible manufacturing systems

(FMS) in those days. He had several Journal and conference papers and books in this area. He was invited by GE R& D centre in Schenectady to give a seminar on FMS, after the seminar the manager of control lab asked him if he can visit their Erie Penn rail engine manufacture plant, probably the first automated factory floor. He designed the control system of the factory. This came in IEEE Robotics and automation as highly cited paper. Later he designed a factory floor control system for a plant in Bangalore.

He developed analysis and design methodologies for six-sigma, integrated manufacturing and service supply chain networks. His research has very strong industrial relevance as well as theoretical rigor. The impact of our research was felt worldwide. The Petri models for manufacturing system performance evaluation and control were formalized in the 80's and several youngsters at that time were inspired to contribute to this important area. He authored a textbook entitled "Performance Modelling of Automated Manufacturing Systems," published by Prentice Hall Inc., USA in 1992. This book is followed worldwide and was reprinted several times as the low-cost editionProfessor Viswanadhamwas editor of manufacturing for IEEE Robotics and Automation. This journal was split into Robotics and TASE. I was EIC of TASE (2008-12). He Started CASE in 2005; The Fifth CASE 2009 was held in Bangalore.

IEEE provides a platform for interaction, service and growth. His service to IEEE started as reviewer, AE, Editor and Editor in Chief; He was member of conference committees, General Chair, Mentor and now on advisory bodies. It is often said that best ideas come from listening to or reading papers in non-related areas. This was indeed true in his case. He was asked to review a paper on Petri nets. He was about to say this is not my area of research but looked at out of curiosity. He found that flexible manufacturing systems can be modelled as using Petri nets and this has led to path breaking research by his team. several papers, PhDs resulted out of this work. His research was followed by others in the field.



Vivek Shripad Borkar Affiliation: IIT Bombay IEEE Fellow Citation: For contributions to stochastic and adaptive control

Bio: Vivek Borkar got his B.Tech. (Elec. Engg.) from IIT Bombay, M.S. (Systems and Control Engg.) from Case Western Reserve Uni., and Ph.D. (Elec. Engg. and Comp. Sci.) from Uni. of California, Berkeley. He has held regular positions at TIFR Centre and Indian Institute of Science in Bengaluru and at Tata Institute of Fundamental Research and Indian Institute of Technology Bombay in Mumbai, where he is now an Emeritus Fellow. He has held visiting positions at TechnischeHogeschool Twente (Holland) and MIT, Uni. of Maryland at College Park, Uni. of California at Berkeley, and Uni. of Illinois at Urbana-Champaign in USA. He is also a fellow of AMS, TWAS, INSA, INAE, IASc, NASI and IETE, and a winner of the S. S. Bhatnagar Prize and TWAS Award, as well as Homi Bhabha, J. C. Bose and S. S. Bhatnagar Fellowships. He was also an invited speaker at the International Congress of Mathematicians in Madrid, 2006.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

- 1. Existence and characterization of optimal controls for Markov decision processes and controlled diffusions with ergodic or risk-sensitive costs, and with constraints.
- 2. Self-tuning adaptive control and control under partial observations of Markov chains and diffusions



Affiliation: IISc Bangalore IEEE Fellow Citation: For contributions to modeling and analysis of manufacturing systems and supply chain networks

Y. Narahari

Bio: Y. Narahari is currently a Professor at the Department of Computer Scienceand Automation, Indian Institute of Science, Bangalore, India. The common thread in his current research is to apply game theory, mechanism design, and artificial intelligence techniques to research problems at the interface of computer science and economics. In particular, he is interested in auctions and markets, cooperative game theory, computational social choice, machine learning, and data analytics.

He is also exploring the application of these to digital agriculture and public health problems. He is the author of a textbook entitled "Game Theory and Mechanism Design" brought out by theIISc Press and the World Scientific Publishing Company and a Co-Author of two other highly cited books. His recognitions include an IISc Award for Research Excellence in Engineering, and Fellowships of INAE, IEEE, INSA, IASc, and NASI, Homi-Bhabha Fellowship, and J.C. Bose National Fellowship.

More details at: http://gtl.csa.iisc.ac.in/hari/.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Factory Modeling and Scheduling: Narahari's work enabled a unified modeling framework to be developed for modeling, analysis, scheduling, and control of large scale manufacturing systems. His modeling approach which unified Petri nets, queueing networks, and other stochastic models is being cited extensively even 30 years after it was proposed. His approach is best documented in the widely acclaimed and widely cited textbook "Performance Modeling of Manufacturing Systems." Six Sigma Supply Chains: Narahari coined the notion of "Six Sigma Supply Chains" to describe supply chain networks with assured levels of performance and provided rigorous methods for designing such supply chain networks.



Yogesh Singh Chauhan Affiliation: IIT Kanpur IEEE Fellow Citation: For contributions to compact modeling of Si and GaN transistors

Bio: Yogesh Singh Chauhan is a professor at Indian Institute of Technology Kanpur, India. He was with Semiconductor Research & Development Center at IBM Bangalore during 2007 – 2010; Tokyo Institute of Technology in 2010; University of California Berkeley during 2010-2012; and ST Microelectronics during 2003-2004. He is the developer of several industry standard models: ASM-GaN-HEMT model, BSIM-BULK (formerly BSIM6), BSIM-CMG, BSIM-IMG, BSIM4 and BSIM-SOI models. His research group is involved in developing compact models for GaN transistors, FinFET, Nanosheet/Gate-All-Around FETs, FDSOI transistors, Negative Capacitance FETs and 2D FETs. His research interests are characterization, modeling, and simulation of semiconductor devices.

He is the Fellow of IEEE and Indian National Academy of Engineering. He is the Editor of IEEE Transactions on Electron Devices and Distinguished Lecturer of the IEEE Electron Devices Society. He is the chair of IEEE-EDS Compact Modeling Committee. He is the founding chairperson of IEEE Electron Devices Society U.P. chapter and chairman-elect of IEEE U.P. section. He has published more than 250 papers in international journals and conferences. He received Ramanujan fellowship in 2012, IBM faculty award in 2013 and P. K. Kelkar fellowship in 2015, CNR Rao faculty award, Humboldt fellowship and Swarnajayanti fellowship in 2018. He has served in the technical program committees of IEEE International Electron Devices Meeting (IEDM), IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), IEEE European Solid-State Device Research Conference (ESSDERC), IEEE Electron Devices Technology and Manufacturing (EDTM), and IEEE International Conference on VLSI Design and International Conference on Embedded Systems.

Details of Contributions responsible for his Elevation to IEEE Fellow Grade:

Dr. Chauhan made sustained and significant impact on the IC industry through his work in Compact Modeling of nanoscale devices. He was the lead researcher in developing a symmetric BSIM compact model for bulk MOSFET to replace the most widely used BSIM4 model. This work resulted in industry standard BSIM-BULK (formerly BSIM6) model for analog and RF circuit design, now adopted at TSMC and other companies for their most advanced planar CMOS technologies.

His compact model for GaN transistors was selected as world's first industry standard model by Compact Model Coalition (CMC) in 2018 after more than five years of rigorous evaluation and is now being used by GaN companies for both power and RF circuit design. GaN transistors are widely used in power electronic systems and RF power applications. He developed several model modules for

different peculiar effects observed in GaN HEMTs such as modules for surface potential, nonlinear access regions, current collapse and gate/drain lag, field-plate capacitance etc. The model is available in major commercial SPICE simulators and is being used widely by GaN companies all over the world. The recent standardization by CMC will make his GaN transistor model a key enabler for above-mentioned applications and their proliferation.

He is also a major contributor to the development of the international industry standard models for FinFETs and FDSOI transistors. Dr. Chauhan is a part of the development team responsible for the industry standard BSIM-CMG model for FinFETs and BSIM-IMG model for FDSOI. He is the lead author of the book titled "FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard" and a co-author of the recently published book "Industry Standard FDSOI Compact Model BSIM-IMG For IC Design".

What distinguishes Dr. Chauhan from many other researchers is that he has worked closely with many foundries, fabless and EDA companies, and international standard organizations over many years to strengthen the industry ecosystem. His distinctly important and exceptionally impactful contributions are embodied in a series of international industry standard compact models of transistors that connects the physics-based foundry/fab world with the computer-based EDA/design world. The models are:

- BSIM-BULK for planar CMOS technology,
- ASM-HEMT for GaN technology,
- BSIM-IMG for FDSOI technology,
- BSIM-CMG for FinFET and Gate-All-Around technologies.

His Compact Modeling research has created a large knowledge base and profoundly enhanced IC industry's capability of designing ever larger and better electronic circuits. His research is widely published as cited in journals such as IEEE IEDM, TED, EDL and TMTT. He has given several invited talks in ESSDERC (2012, 2016) and WCM (2011, 2012, 2014, 2018) etc. He has particularly introduced compact modeling to a vast number of young researchers in India through short courses, tutorials, distinguished lectures and workshops making a strong social impact in India while making India a world leader is compact modeling research.